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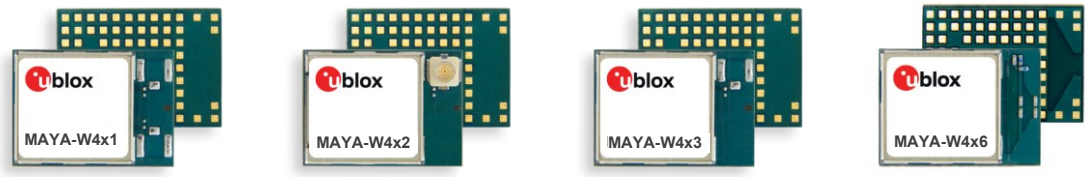
MAYA-W4 series

Host-based multiradio modules with Wi-Fi 6, Bluetooth® Low Energy, and IEEE 802.15.4

Data sheet



Abstract

Targeted towards system integrators and design engineers, this technical data sheet includes the functional description, pin definition, specifications, country approval status, handling instructions, and ordering information for MAYA-W4 short-range radio modules.

This range of ultra-compact, cost-efficient, host-based, short range multiradio modules support tri-radio Wi-Fi 6, Bluetooth Low Energy, and IEEE 802.15.4 connectivity. The modules are designed for a wide range of industrial applications and are supplied with or without an internal antenna. Integrated with a MAC/Baseband processor and RF front end components, this module series connects to a host processor through various interfaces, including SDIO or USB for Wi-Fi, High-Speed UART or USB for Bluetooth, and SPI for 802.15.4.

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Product status	Corresponding content status	
Functional sample	Draft	For functional testing. Revised and supplementary data will be published later.
In development / Prototype	Objective specification	Target values. Revised and supplementary data will be published later.
Engineering sample	Advance information	Data based on early testing. Revised and supplementary data will be published later.
Initial production	Early production information	Data from product verification. Revised and supplementary data may be published later.
Mass production / End of life	Production information	Document contains the final product specification.

This document applies to the following products:

Product name	Type number	Product status
MAYA-W433	MAYA-W433-00B-00	Engineering Sample
MAYA-W436	MAYA-W436-00B-00	Engineering Sample
MAYA-W442	MAYA-W442-00B-00	In development
MAYA-W463	MAYA-W463-00B-00	Engineering Sample
MAYA-W466	MAYA-W466-00B-00	Initial Production
MAYA-W471	MAYA-W471-00B-00	In development
MAYA-W472	MAYA-W472-00B-00	In development
MAYA-W473	MAYA-W473-00B-00	Engineering Sample
MAYA-W476	MAYA-W476-00B-00	Initial Production

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Contents

1 Functional description

1.1 Overview

The MAYA-W4 series host-based modules are designed, built, and tested to meet the high reliability and quality requirements of industrial and commercial applications, such as building automation, professional appliances, energy management, smart homes, healthcare, and more.

MAYA-W4 modules provide SISO Wi-Fi 6 operation with 20 MHz channel width and improved network availability in dense Wi-Fi environments. The modules can work as an access point, station, in P2P connections, or combinations of these.

MAYA-W4 supports Bluetooth® Low Energy (LE), including the use of isochronous channels for LE Audio. MAYA-W44x and -W47x variants support an IEEE 802.15.4 radio for Thread mesh network support. The Matter application protocol is supported over Thread and Wi-Fi allowing interoperability with various products in a growing ecosystem.

At 10.4 x 14.3 mm, MAYA-W4 are among the most compact Wi-Fi 6 SMD modules with integrated antenna or U.FL connector.

All u-blox modules undergo extensive qualification tests to ensure reliability over their lifetime, and each module is fully tested before leaving the assembly line. The modules are verified against Bluetooth Core 5.4.

The MAYA-W4 series is based on the NXP IW610 chipset family.

Key features

- Variants with antenna pin(s), U.FL connector, and embedded PCB antenna
- Wi-Fi 6, single- and dual-band, single stream, supporting MU-MIMO, 20 MHz channels
- Wi-Fi 802.11a/b/g/n/ac/ax - e/i/k/r/v/w
- Wi-Fi security: WPA3, WPA2, AES
- Bluetooth Low Energy 5.4 supporting LE Audio
- 802.15.4 radio for Thread
- Secure operation (Edgelock™), secure boot
- Industrial temperature range –40 °C to +85 °C

1.2 Product features

Radio features	Description
Chipset	NXP IW610x
Variants	MAYA-W47x: Dual-band 2.4/5 GHz Wi-Fi 6 + Bluetooth LE/802.15.4 MAYA-W46x: Dual-band 2.4/5 GHz Wi-Fi 6 + Bluetooth LE MAYA-W44x: Single-band 2.4 GHz Wi-Fi 6 + Bluetooth LE/802.15.4 MAYA-W43x: Single-band 2.4 GHz Wi-Fi 6 + Bluetooth LE
Wi-Fi Standards	1x1 dual-band Wi-Fi 6, IEEE 802.11a/b/g/n/ac/ax, 20 MHz channel operation
Wi-Fi frequency bands	2.4 GHz, channel 1-13 5 GHz, channel 36-177
Bluetooth Low Energy	Bluetooth Low Energy 5.4 specification support
802.15.4	IEEE 802.15.4-2015 compliant; supports Matter over Thread in 2.4 GHz band
Antenna configurations	Dual antenna pin for simultaneous Wi-Fi and Bluetooth Low Energy/802.15.4 operation
	Single antenna pin or U.FL connector for shared 2.4 GHz Wi-Fi and Bluetooth Low

Radio features	Description
	Energy/802.15.4 operation
	Internal antenna for shared 2.4 GHz Wi-Fi and Bluetooth Low Energy/802.15.4 operation
Software features	
Security	WPA3, WPA2, and WPA mixed mode
RF calibration and MAC addresses	Available in on-board OTP memory
Wi-Fi operational modes	Station, Access Point, Wi-Fi direct, or in a combination of these modes
Driver support	Free drivers for Linux and Android. RTOS (with certain types of NXP MCUs)
Interfaces	
Wi-Fi	SDIO 3.0 (4-bit, up to 208 MHz clock) or USB 2.0
Bluetooth Low Energy	4-wire high-speed UART (HCI transport layer) or USB 2.0
802.15.4	SPI (up to 10 MHz clock)
Other	GPIOs, Coexistence interfaces
Package	
Dimensions	10.4 x 14.3 x 2.0 mm
Mounting	Soldering, 90 pins (LGA)
Environmental data, quality, and reliability	
Operating temperature	-40 °C to +85 °C (Professional Grade)
Moisture Sensitivity Level (MSL)	4
RoHS and REACH compliance	Yes
Electrical data	
Module power supply	3.3 VDC and 1.8 VDC
I/O power supply	3.3 VDC or 1.8 VDC
Certifications and approvals	
Type approvals	Europe (RED), US (FCC), Canada (ISED), United Kingdom (UKCA), Japan (Giteki). See Qualifications and approvals. Other country certifications can be provided on request.
Bluetooth qualification	Bluetooth Core 5.4
Support products	
EVK-MAYA-W476	Evaluation kit for MAYA-W476, -W473
EVK-MAYA-W471	Evaluation kit for MAYA-W471

Table 1: MAYA-W4 series product features

☞ For information about the supported MAYA-W4 series product variants, see Ordering information.

1.3 Block diagrams

MAYA-W4 module variants with an internal antenna support a single RF pin and an optional antenna feed pin (**ANT_FEED**) to the internal PCB antenna. For information about the various antenna configurations for MAYA-W4 series module, see also Antenna interfaces.

Single antenna configurations support:

- Time-shared 2.4 GHz Wi-Fi and Bluetooth Low Energy/802.15.4 operation
- Simultaneous 5 GHz Wi-Fi and Bluetooth Low Energy/802.15.4 operation
- Bluetooth Low Energy/802.15.4 operation is always time-shared

Figure 1 shows the block diagram of the single antenna variants in the MAYA-W4 series, which support either a single antenna pin, U.FL connector, or internal antenna.

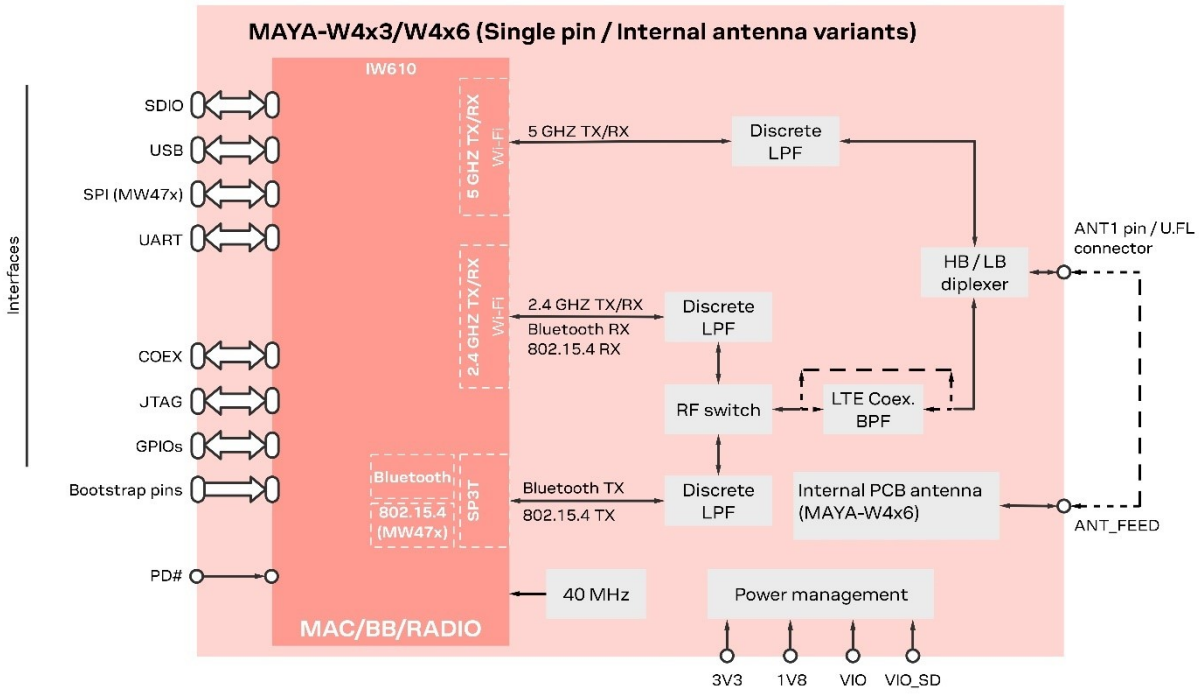


Figure 1: Block diagram of MAYA-W4 single pin, single U.FL, and internal antenna variants

Figure 2 shows the block diagram of the dual pin variants of the MAYA-W4 series. The dual antenna configurations support simultaneous Wi-Fi and time-shared Bluetooth Low Energy/802.15.4 operation.

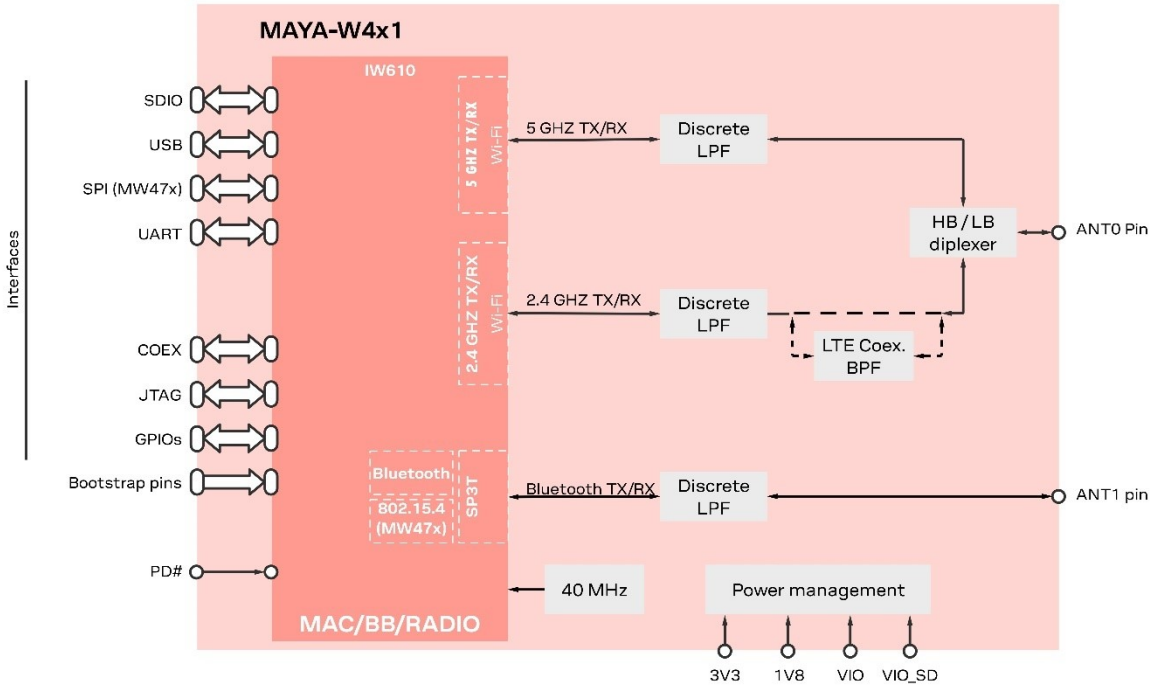


Figure 2: Block diagram of MAYA-W4 dual pin variants

1.4 Product description

MAYA-W4 series comprises ultra-compact Wi-Fi front-end modules with a footprint of only 14.3 x 10.4 mm. The modules are developed for reliable, high-performance, industrial devices and applications.

Based on the NXP IW610x chipset family, MAYA-W4 includes an integrated MAC/Baseband processor and RF front-end components. The MAYA-W4 series supports variants with single- or dual-band Wi-Fi 6, Bluetooth Low Energy 5.4, and optional 802.15.4 radio.

All module variants support:

- Integrated discrete filters in the 2.4 GHz band and 5 GHz band
- Optional LTE filter for improved coexistence with LTE bands 7, 38, 40, 41

1.5 Supported features

- Highly effective internal antenna, antenna pin(s), or U.FL connector
- Extended operating temperature range of -40 °C to +85 °C for professional grade
- Selectable 1.8 V or 3.3 V I/O levels
- Selectable SDIO voltage levels
- Internal Wi-Fi/Bluetooth Low Energy/802.15.4 coexistence support
- External coexistence interfaces for connection to external radios such as LTE
- IEC-62443 cyber-security compliance
- Authenticated and secured boot

1.5.1 Wi-Fi features

- Supports Wi-Fi 6, IEEE 802.11 a/b/g/n/ac/ax
- Dual-band 2.4 GHz or 5 GHz Wi-Fi 6 radio
- Single stream 1x1 802.11ax with 20 MHz channel bandwidth
- PHY data rate up to 115 Mbit/s (802.11ax: MCS0-9, 802.11ac: MCS0-8, 802.11n: MCS0-7)
- 802.11n short and long guard interval
- Wi-Fi 6 Extended Range (ER) and Dual Carrier Modulation (DCM)
- Power saving features, Wi-Fi 6 Target Wake Time (TWT) support
- Host interfaces: SDIO 3.0 or USB 2.0 device
- Security: WPA3, WPA2 and WPA mixed mode, 802.1X
- Wi-Fi Standards IEEE 802.11e/i/k/r/v/w
- Supports simultaneous station, access point and P2P modes
- Supports up to eight stations in AP mode
- Matter over Wi-Fi
- Antenna diversity

1.5.2 Bluetooth Low Energy features

- Bluetooth Low Energy 5.4 specification support
- Bluetooth Low Energy Class 1 and Class 2 operation
- Bluetooth Low Energy Long range (125/500 kbps)
- Bluetooth Low Energy 1 and 2 Mbit/s PHY
- Isochronous channels (ISOC) supporting Bluetooth Low Energy Low Energy (LE) audio
- Host interfaces: High-speed UART with standard HCI transport layer or USB 2.0 device
- Encryption (AES) support
- Bluetooth Low Energy Broadcaster, Observer, Central, and Peripheral roles
- Bluetooth Low Energy Link layer topology (connects up to 16 links)
- Bluetooth Low Energy Privacy 1.2
- Bluetooth Low Energy Secure connection
- Bluetooth Low Energy Data length and advertising extension
- Bluetooth Low Energy Power control

1.5.3 802.15.4 features

- IEEE 802.15.4-2015 compliant supporting Matter over Thread in 2.4 GHz band
- Shared transmitter and antenna pin with Bluetooth Low Energy
- Simultaneous receive with Wi-Fi and Bluetooth Low Energy
- MAC accelerator with packet formatting, CRCs, address check, auto-acks, timers
- Received signal strength indication (RSSI) of received packets
- 128-bit AES security
- SPI host interface with maximum clock speed of 10 MHz

1.6 Reserved MAC addresses

MAYA-W4 series modules have four consecutive MAC addresses that are unique for each module variant. The first three of these four addresses are configured during production.

The first address is used for the Bluetooth Low Energy communication, while the second address is configured for Wi-Fi communication. The third address is extended to a 64-bit MAC address by inserting two 00-hex bytes and used for the 802.15.4 radio. The Data Matrix Code shown on the product label includes the Bluetooth Low Energy MAC address. See also Product labeling. The remaining MAC address is not used in the manufacturing configuration but is reserved for module usage.

MAC address	Assignment	Last two bits of MAC address	Example
Module1, address 1	Bluetooth Low Energy	00	D4:CA:6E:44:00:04
Module1, address 2	Wi-Fi	01	D4:CA:6E:44:00:05
Module1, address 3	802.15.4	10	D4:CA:6E:00:00:44:00:06
Module1, address 4	(free for use)	11	D4:CA:6E:44:00:07
Module2, address 1	Bluetooth Low Energy	00	D4:CA:6E:44:00:08
Module2, address 2	Wi-Fi	01	D4:CA:6E:44:00:09
Module2, address 3	802.15.4	10	D4:CA:6E:00:00:44:00:0A
Module2, address 4	(free for use)	11	D4:CA:6E:44:00:0B

Table 2: MAC address assignment

2 Interfaces

2.1 Interface configuration

MAYA-W4 supports three configuration pins **CON[0:2]** for selecting the host interface configuration, as shown in Table 3. Additional configuration pins are required to set configuration parameters following a hardware reset, as described in Table 4. Configuration pins revert to their usual function immediately after the reset.

To set a configuration bit to 0, attach a 51 kΩ resistor from the pin to ground. No external circuitry is required to set a configuration bit to 1, except on **CON[2]**.

CON[2:0]	Wi-Fi	Bluetooth Low Energy	802.15.4
011 (default)	SDIO	UART	SPI
101	USB	USB	SPI
Others	Reserved	Reserved	Reserved

Table 3: Firmware boot options

Configuration bits	Pin name	Configuration function
CON[5]	RF_CNTL0 / CONFIG_XOSC_SEL	Reference clock frequency selection. Must be set to 1 or leave open.
CON[3]	CON[3]	Reserved. Set to 1 or leave open.
CON[2:0]	CON[2:0]	Host configuration options. Selects the host interface used for Wi-Fi, Bluetooth Low Energy, and 802.15.4 radio. 011 = (default). See Table 3.

Table 4: Configuration pins

2.2 Host interfaces

MAYA-W4 supports the following host interfaces:

- SDIO 3.0 and USB 2.0 device interface for Wi-Fi
- High-speed UART and USB 2.0 device interface for Bluetooth Low Energy
- SPI interface for 802.15.4 radio

The host interfaces are selected using the configuration pins described in Table 3.

2.2.1 SDIO interface

MAYA-W4 supports an SDIO device interface that conforms to the industry standard SDIO 3.0 specification, including default speed (25 MHz), high-speed (50 MHz), SDR12/25/50/104 (12/25/50/104 MB/s), and DDR50 (50 MB/s) modes. The interface supports 1-bit and 4-bit SDIO transfer modes at the full clock range up to 208 MHz for SDR104. All mandatory SDIO commands are supported.

In 4-bit SDIO mode, data is transferred on all four data pins (**SD_DAT**[3:0]). The interrupt pin is not available for exclusive use as it is utilized as a data transfer line. If the interrupt function is required, special timing is required to provide interrupts. The 4-bit SDIO mode provides the highest data transfer possible with speeds up to 104 MB/s in SDR104 mode.

The pull-up resistors required for the SD interface on **SD_CMD**, **SD_DAT**[3:0] must be provided by the host. The value of resistors should be between 10–100 kΩ.

Low value series termination resistors can be required to help with signal integrity. The SDIO signals levels are selectable according to the **VIO_SD** 1.8/3.3 voltage levels (depending on SDIO mode selection). See Power supply interfaces.

Table 5 describes the required pins for the SDIO interface.

Pin name	I/O type	1-bit mode	4-bit mode
SD_DAT[0]	I/O	Data line	Data line 0
SD_DAT[1]	I/O	Interrupt	Data line 1
SD_DAT[2]	I/O	Read Wait (optional)	Data line 2
SD_DAT[3]	I/O	Not used	Data line 3
SD_CMD	I/O	Command line	Command line
SD_CLK	I	Clock input	Clock input

Table 5: SDIO interface pin description

2.2.1.1 Default speed and high-speed modes (3.3 V)

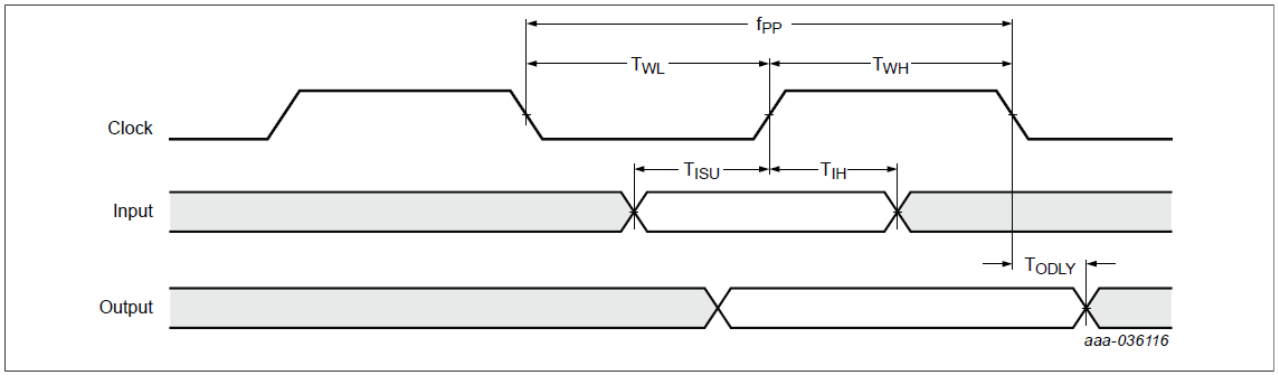


Figure 3: SDIO protocol timing diagram - default speed mode

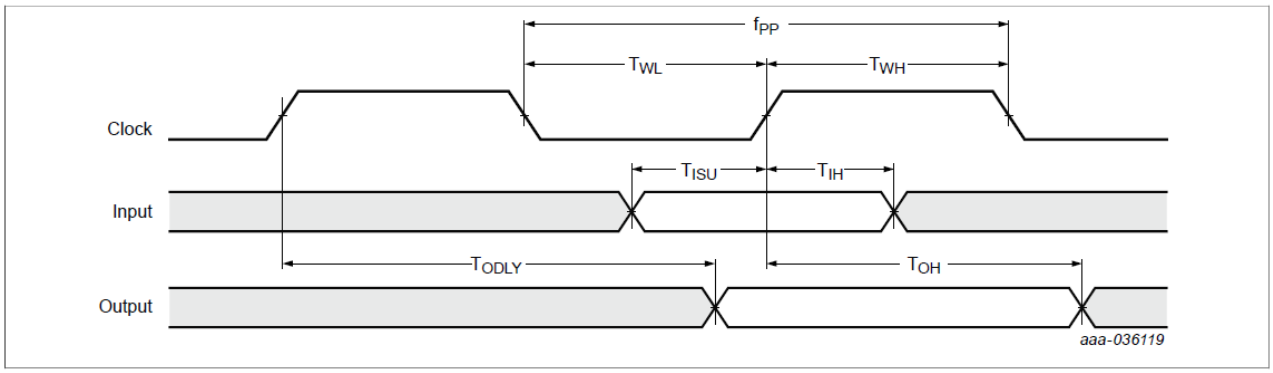


Figure 4: SDIO protocol timing diagram – high speed mode

Table 6 describes the SDIO timing data for the default and high-speed modes with the SDIO clock running at 25 MHz or 50 MHz.

Symbol	Parameter	Condition	Min	Typ	Max	Unit
f_{pp}	Clock frequency	Default speed	0	-	25	MHz
		High speed	0	-	50	MHz
T_{WL}	Clock low time	Default speed	10	-	-	ns
		High speed	7	-	-	ns
T_{WH}	Clock high time	Default speed	10	-	-	ns
		High speed	7	-	-	ns
T_{ISU}	Input setup time	Default speed	5	-	-	ns

Symbol	Parameter	Condition	Mln	Typ	Max	Unit
		High speed	6	-	-	ns
T_{IH}	Input hold time	Default speed	5	-	-	ns
		High speed	2	-	-	ns
T_{ODLY}	Output Delay Time	Default speed	-	-	14	ns
		High speed	-	-	14	ns
T_{OH}	CL≤40 pF (1 card)	Default speed	2.5	-	-	ns
		High speed	-	-	-	ns

Table 6: SDIO timing data – default and high-speed modes

2.2.1.2 SDR12, SDR25, SDR50 modes (up to 100 MHz) (1.8 V)

Table 7 describes the SDIO timing data for the SDR12/25/50 modes with the SDIO clock running at up to 100 MHz. The **VIO_SD** power pin must be supplied at 1.8 V.

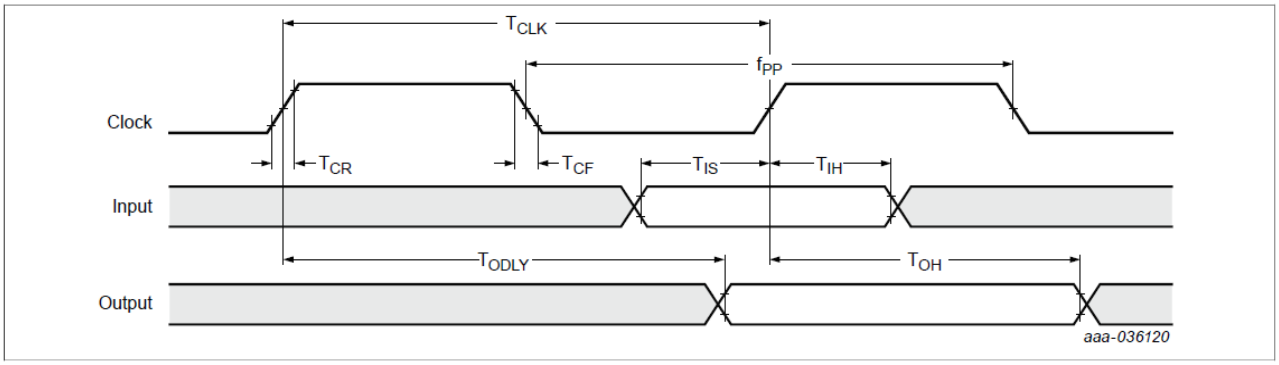


Figure 5: SDIO protocol timing diagram – SDR12, SDR25, SDR50 modes (up to 100 MHz) (1.8 V)

Symbol	Parameter	Condition	Min	Typ	Max	Unit
f_{pp}	Clock frequency	SDR 12	0	–	25	MHz
		SDR 25	0	-	50	
		SDR 50	0	-	100	
T_{IS}	Input setup time	SDR 12	5	–	–	ns
		SDR 25	6	-	-	
		SDR 50	3	-	-	
T_{IH}	Input hold time	SDR 12	5	–	–	ns
		SDR 25	2			
		SDR 50	0.8			
T_{CLK}	Clock time	SDR 12	40	–	40	ns
		SDR 25	10	-	20	
		SDR 50	10	-	10	
T_{CR} ,T_{CF}	Rise time, fall time T_{CR} ,T_{CF} < 2 ns (max) at 100 MHz C_{CARD} = 10 pF	SDR 12	–	–	0.2*T_{CLK}	ns
		SDR 25	–	–	0.2*T_{CLK}	ns
		SDR 50	–	–	0.2*T_{CLK}	ns
T_{OLDY}	Output delay time C_L ≤ 30 pF	SDR 12	–	–	7.5	ns
		SDR 25	–	–	14	ns
		SDR 50	–	–	14	ns
T_{OH}	Output hold time C_L = 15 pF	SDR 12	1.5	–	–	ns
		SDR 25	1.5	–	–	ns
		SDR 50	1.5	–	–	ns

Table 7: SDIO timing data – SDR12, SDR25, SRD50 modes (up to 100 MHz) (1.8 V)

2.2.1.3 DDR50 mode (50 MHz) (1.8 V)

Table 8 describes the SDIO timing data for the DDR50 mode with the SDIO clock running at 50 MHz. The **VIO_SD** power pin must be supplied at 1.8 V.

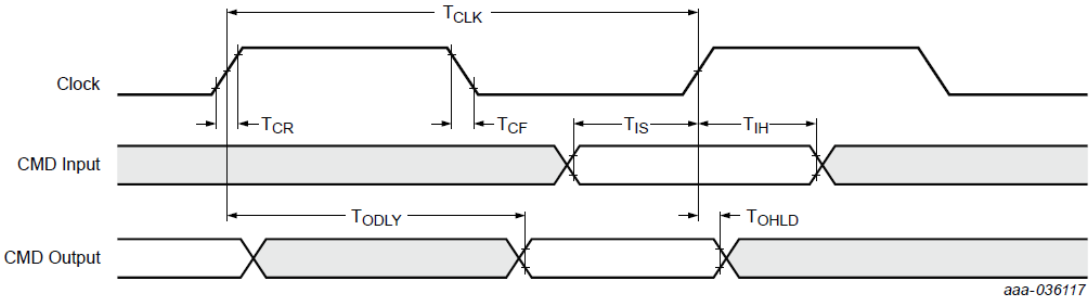


Figure 6: SDIO CMD timing diagram – DDR50 mode (50 MHz)

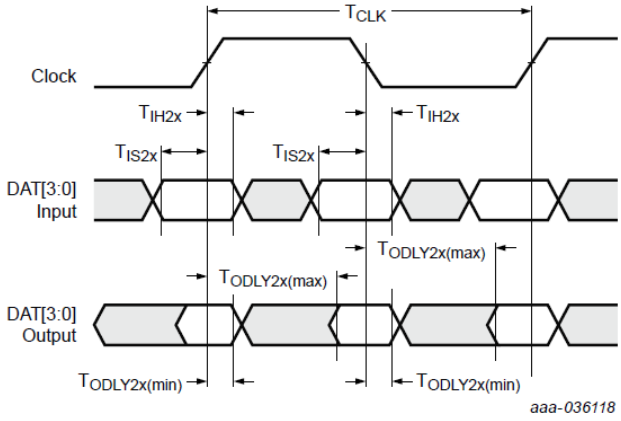


Figure 7: SDIO DAT[3:0] timing diagram – DDR50 mode

Symbol	Parameter	Condition	Min	Typ	Max	Unit
Clock						
T_{CLK}	Clock time 50 MHz (max) between rising edges	DDR 50	20	–	–	ns
T_{CR} ,T_{CF}	Rise time, fall time T_{CR} ,T_{CF} < 4.00 ns (max) at 50 MHz C_{CARD} = 10 pF	DDR 50	–	–	0.2*T_{CLK}	ns
Clock duty	–	DDR 50	45	–	55	%
CMD input (with reference to rising clock edge)						
T_{IS}	Input setup time C_{CARD} = 10 pF (1 card)	DDR 50	6	–	–	ns
T_{IH}	Input hold time C_{CARD} = 10 pF (1 card)	DDR 50	0.8	–	–	ns
CMD output (referenced to clock rising edge)						
T_{ODLY}	Output delay time during data transfer mode $C_L \leq$ 30 pF (1 card)	DDR 50	–	–	13.7	ns
T_{OHLD}	Output hold $C_L \geq$15 pF (1 card)	DDR 50	1.5	–	–	ns
DAT[3:0] Input (referenced to clock rising and falling edges)						
T_{IS2x}	Input setup time $C_{CARD} \leq$10 pF (1 card)	DDR 50	3	–	–	ns
T_{IH2x}	Input hold time	DDR 50	0.8	–	–	ns

Symbol	Parameter	Condition	Min	Typ	Max	Unit
	$C_{CARD} \leq 10$ pF (1 card)					
DAT[3:0] Output (referenced to clock rising and falling edges)						
T_{ODLY2x} (max)	Output delay time during data transfer mode $C_L \leq 25$ pF (1 card)	DDR 50	–	–	7.0	ns
T_{ODLY2x} (min)	Output hold time $C_L \geq 15$ pF (1 card)	DDR 50	1.5	–	–	ns

Table 8: SDIO timing data – DDR50 mode (50 MHz)

2.2.1.4 SDR104 mode (208 MHz) (1.8 V)

Table 9 describes the SDIO timing data for the SDR104 mode with SDIO clock running at 208 MHz. The **VIO_SD** power pin must be supplied at 1.8 V.

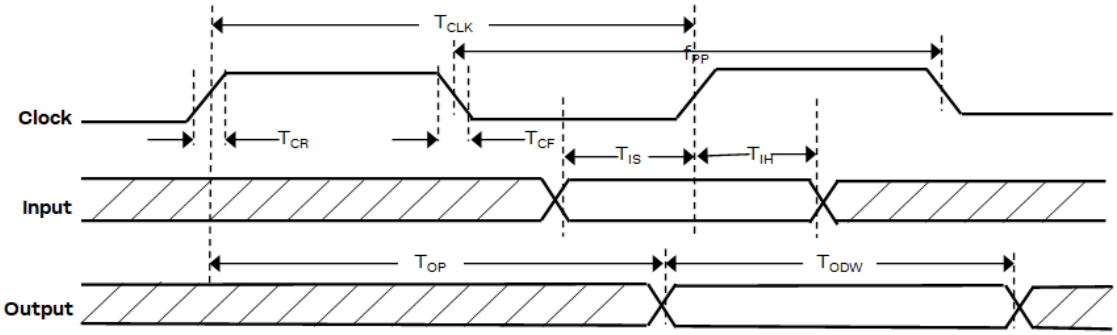


Figure 8: SDIO DAT[3:0] timing diagram – SDR104 mode

Symbol	Parameter	Condition	Min	Typ	Max	Unit
f_{PP}	Clock frequency	SDR104	0	-	208	MHz
T_{IS}	Input setup time	SDR104	1.4	–	–	ns
T_{IH}	Input hold time	SDR104	0.8	–	–	ns
T_{CLK}	Clock time	SDR104	4.8	–	–	ns
T_{CR}, T_{CF}	Rise time, fall time T_{CR}, T_{CF} < 0.96 ns (max) at 208 MHz C_{CARD} = 10 pF	SDR104	--	--	0.2*T_{CLK}	ns
T_{OP}	Card output phase	SDR104	0	–	2	ns
T_{ODW}	Output timing of variable data window	SDR104	2.88	–	–	ns

Table 9: SDIO timing data – SDR104 mode (208MHz)

2.2.1.5 SDIO internal pull-up and pull-down specifications

Parameter	Condition	Min	Typ	Max	Unit
Internal nominal pull-up/pull-down resistance		70	100	140	kΩ

Table 10: SDIO internal pull-up and pull-down specifications

2.2.2 USB interface

The USB device interface is compliant with the *Universal Serial Bus Specification, Revision 2.0, April 27, 2000*.

The USB device interface supports:

- Low speed (1.5 Mbps), full speed (12 Mbps), high speed (480 Mbps) operation
- Link Power Management (LPM), corresponding host resume, or device resume (remote wakeup) to exit from L1 sleep state

Signals	Symbol	Parameter	Min	Typ	Max	Unit
USB power valid indication	V_{VBUSIL}	USB_VBUS_ON LOW level input voltage	-0.4	-	0.3*VIO	
	V_{VBUSIH}	USB_VBUS_ON HIGH level input voltage	0.7*VIO	-	VIO+0.4	
Input levels for Low Speed and Full Speed	V_{IL}	Low level input voltage	-	-	0.8	V
	V_{IH}	High level input voltage (driven)	2.0	-	-	V
	V_{DI}	Differential input sensitivity	0.2	-	-	V
	T_{JR1}	Receiver Jitter to next transition (Full speed)	-18.5	-	18.5	ns
	T_{JR2}	Receiver Jitter for paired transitions (Full speed)	-9.0	-	9.0	ns
Output levels for Low Speed	V_{OL}	Low level output voltage	0	-	0.3	V
	V_{OH}	High level output voltage (driven)	2.8	-	3.6	V
	V_{CRS}	Output signal crossover voltage	1.3	-	2.0	V
	T_{LR}	Data fall time	75.0	-	300.0	ns
	T_{LF}	Data rise time	75.0	-	300.0	ns
	T_{LRFM}	Rise and fall time matching	80.0	-	125.0	%
	T_{UDJ1}	Source jitter total to next transition	-95.0	-	95.0	ns
	T_{UDJ2}	Source jitter total for paired transitions	-150.0	-	150.0	ns
Output levels for Full Speed	V_{OL}	Low level output voltage	0	-	0.3	V
	V_{OH}	High level output voltage (driven)	2.8	-	3.6	V
	V_{CRS}	Output signal crossover voltage	1.3	-	2.0	V
	T_{FR}	Output rise time	-4.0	-	20.0	ns
	T_{FL}	Output fall time	-4.0	-	20.0	ns
	T_{DJ1}	Source jitter total to next transition	-3.5	-	3.5	ns
	T_{DJ2}	Source jitter total for paired transitions	-4.0	-	4.0	ns
	T_{FDEOP}	Source jitter for diff. transition to SE0 transition	-2.0	-	5.0	ns
Input Levels for High Speed	V_{HSSQ}	High-speed squelch detection threshold (differential signal amplitude)	100	-	150	mV
	V_{HSDSC}	High-speed disconnect detection threshold (differential signal amplitude)	525	-	625	mV
	V_{HSCM}	High-speed data signaling common mode voltage range	-50	-	500	mV
Output Levels for High Speed	V_{HSOH}	High-speed data signaling high	360	-	440	mV
	V_{HSOL}	High-speed data signaling low	-10	-	10	mV
	T_{HSR}	Data rise time	500	-	-	ns
	T_{HSF}	Data fall time	-500	-	-	ns
Data rate	T_{LSDRAT}	Low speed data rate	-	1.5	-	Mb/s
	T_{FSDRAT}	Full speed data rate	-	12	-	Mb/s
	T_{HSDRAT}	High speed data rate	-	480	-	Mb/s

Table 11: USB characteristics

2.2.3 UART interface

MAYA-W4 supports a high-speed UART host interface for Bluetooth Low Energy operation with a baud rate of up to 4.0 Mbit/s. The default baud rate after reset is 115.2 Kbps and the acceptable deviation from the UART Rx target baud rate is ±3%. The UART supports RX/TX pins and mandatory RTS/CTS flow control signals.

Table 12 describes the module pins for the UART interface.

Pin name	I/O type	Description	GPIO pin multiplexing
UART_CTS	I	Active low clear-to-send input signal	GPIO[12]
UART_TX	O	UART serial output signal	GPIO[15]
UART_RX	I	UART serial input signal	GPIO[14]
UART_RTS	O	Active low request-to-send signal	GPIO[13]

Table 12 Bluetooth Low Energy UART interface description

2.2.4 SPI interface

An SPI host interface is supported for the 802.15.4 radio with a maximum clock speed of 10 MHz. Table 13 describes the module pins for the SPI interface.

Pin name	I/O type	Description	GPIO pin multiplexing
SPI_FRM	I	SPI frame input signal (chip select), active low	GPIO[8]
SPI_CLK	I	SPI clock input signal	GPIO[9]
SPI_RX	I	SPI receive input signal	GPIO[7]
SPI_TX	O	SPI transmit output signal	GPIO[6]

Table 13: 802.15.4 SPI interface description

2.3 Antenna interfaces

All MAYA-W4 variants support a switching antenna diversity solution for Wi-Fi through RF control of an external antenna switch. The switch is controlled by the **RF_CNTL3** signal from the module. For more information about antenna switch design, see also the system integration manual [2].

The MAYA-W4 series supports multiple single- and dual-antenna configurations:

- Single internal antenna or antenna pin – configured externally by a 0 Ω jumper
- Single external antenna connected through antenna pin or on-module U.FL connector
- Two external antennas connected through antenna pins

To prevent mutual interference and improve coexistence performance with LTE bands, MAYA-W4 supports an optionally integrated, high-performance 2.4 GHz SAW LTE band pass filter.

Table 14 shows the available antenna configurations on MAYA-W4 series modules.

Product name	Antenna interface	Description
MAYA-W433	RF_ANT1	Antenna pin for external 2.4 GHz Wi-Fi and Bluetooth Low Energy antenna. Bluetooth Low Energy and 2.4 GHz Wi-Fi are time-shared.
MAYA-W436	RF_ANT1	Antenna pin for external 2.4 GHz Wi-Fi and Bluetooth Low Energy antenna. Bluetooth Low Energy and 2.4 GHz Wi-Fi are time-shared.
	ANT_FEED	External antenna feed pin from RF_ANT1 for internal PCB antenna
MAYA-W442	U.FL	U.FL connector for external 2.4 GHz Wi-Fi, Bluetooth Low Energy, and 802.15.4 antenna. Bluetooth Low Energy, 802.15.4, and 2.4 GHz Wi-Fi are time-shared.
MAYA-W463	RF_ANT1	Antenna pin for external 2.4/5 GHz Wi-Fi and Bluetooth Low Energy antenna. Bluetooth Low Energy and 2.4 GHz Wi-Fi are time-shared.
MAYA-W466	RF_ANT1	Antenna pin for external 2.4/5 GHz Wi-Fi and Bluetooth Low Energy antenna. Bluetooth Low Energy and 2.4 GHz Wi-Fi are time-shared.

Product name	Antenna interface	Description
	ANT_FEED	External antenna feed pin from RF_ANT1 for internal PCB antenna
MAYA-W471	RF_ANT0	Antenna pin for external 2.4/5 GHz Wi-Fi antenna
	RF_ANT1	Antenna pin for external Bluetooth Low Energy/802.15.4 antenna
MAYA-W472	U.FL	U.FL connector for external 2.4/5 GHz Wi-Fi, Bluetooth Low Energy, and 802.15.4 antenna. Bluetooth Low Energy, 802.15.4, and 2.4 GHz Wi-Fi are time-shared.
MAYA-W473	RF_ANT1	Antenna pin for external 2.4/5 GHz Wi-Fi, Bluetooth Low Energy, and 802.15.4 antenna. Bluetooth Low Energy, 802.15.4, and 2.4 GHz Wi-Fi are time-shared.
MAYA-W476	RF_ANT1	Antenna pin for external 2.4/5 GHz Wi-Fi, Bluetooth Low Energy, and 802.15.4 antenna. Bluetooth Low Energy, 802.15.4, and 2.4 GHz Wi-Fi are time-shared.
	ANT_FEED	External antenna feed pin from RF_ANT1 for internal PCB antenna

Table 14: MAYA-W4 antenna configurations

2.3.1 Internal antenna

MAYA-W4 variants with internal antenna have an internal (on-board niche) 2.4/5 GHz antenna that is specifically designed and optimized for the MAYA form factor. The module has an RF signal pin (**RF_ANT1**) and an antenna feed pin for the internal antenna (**ANT_FEED**), so it is possible to use either an external antenna connected to **RF_ANT1**, or the internal antenna by connecting **RF_ANT1** to the **ANT_FEED** pin.

2.3.2 External RF antenna interface

MAYA-W4 variants that are equipped with RF pins (**RF_ANT0**, **RF_ANT1**) or a U.FL connector provide antenna interfaces with a 50 Ω characteristic impedance for use with external antennas. The external antenna can be an SMD antenna (or PCB integrated antenna) mounted on the host board. An antenna connector for use with an external antenna through a coaxial cable can also be considered. The use of a cable antenna can be necessary if the module is mounted in a shielded enclosure, such as a metal box or cabinet. For the list of approved antennas, see the MAYA-W4 system integration manual [2].

2.4 Power supply interfaces

The DC power for MAYA-W4 series modules is supplied through **3V3**, **1V8**, **VIO** and **VIO_SD** pins. The separate **VIO** pin enables the integration of MAYA-W4 in either 1.8 V or 3.3 V applications without the need for level converters. **VIO_SD** is used for digital 1.8 V/3.3 V SDIO power supply.

2.4.1 Power up sequence timing

The module has no power up-sequence requirements. The power-down (**PDn**) pin must be held low (asserted) until all external power supply rails are stable, see Figure 9. T_{PU_RESET} is defined in Table 15.

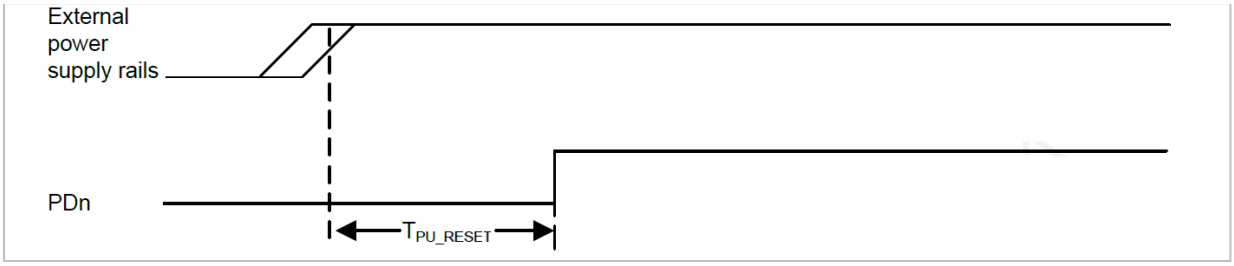


Figure 9: Power-up sequence for MAYA-W4 module

2.4.2 Power down

MAYA-W4 series modules can be put into a low-leakage power mode when the radios are not in use. To do this, assert **PDn** low to enter power-down mode. Firmware download is required again after exiting power-down mode. If the firmware is not downloaded, the device must be kept in power-down mode to reduce leakage. Alternatively, **3V3**, **1V8**, **VIO** and **VIO_SD** can be powered off. In this case, the state of the **PDn** pin becomes irrelevant. See Figure 10.

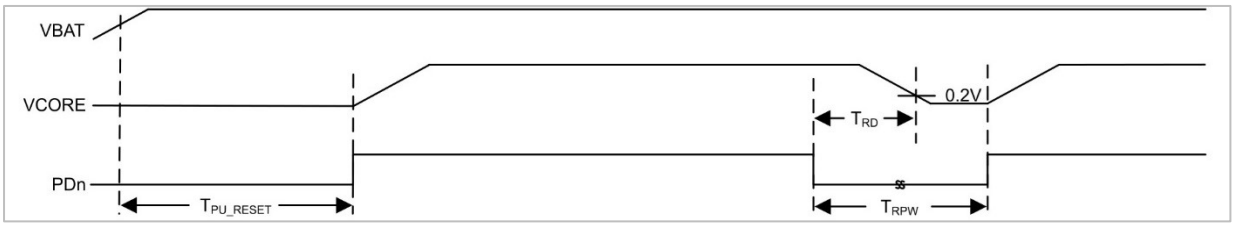


Figure 10: Power-down (PDn) timing

Symbol	Parameter	Condition	Min	Typ	Max	Unit
T_{PU_RESET}	Valid power to PDn deasserted	-	0	-	-	ms
T_{RPW}	PDn pulse width	-	T_{RD} [1]	-	-	us
V_{IH}	Input high voltage	-	1.75	-	3.63	V
V_{IL}	Input low voltage	-	-0.4	-	0.2	V

Table 15: PDn pin specifications

[1] Minimum value guaranteed for a valid reset is 10 us (preliminary). Smaller values may put the device in an undefined state.

2.4.3 Reset

MAYA-W4 series is reset when **PDn** is asserted low (< 0.2 V) and transitions from low to high while power supplies remain active.

2.5 Wake-up and reset interfaces

A deep-sleep mode in MAYA-W4 is used to reduce power consumption. Table 16 shows optional out-of-band wake-up pins to wake up the radios from sleep mode. Radio-to-host, wake-up output signals can be used to wake up the host from sleep mode.

Pin name	I/O type	Description	GPIO pin multiplexing
WL_WAKE_OUT	O	Wi-Fi radio wake-up output signal	GPIO[4]
WL_WAKE_IN	I	Wi-Fi radio wake-up input signal	GPIO[16]
NB_WAKE_OUT	O	Bluetooth LE/802.15.4 radio wake-up output signal	GPIO[5]
NB_WAKE_IN	I	Bluetooth LE/802.15.4 radio wake-up input signal	GPIO[17]
SPI_INT	O	SPI interrupt output signal	-
SD_INT	O	Optional SDIO interrupt output signal	GPIO[1]

Table 16: Wake-up pins

Software reset pins can be used to independently reset the Wi-Fi and Bluetooth Low Energy/802.15.4 radios in MAYA-W4.

Pin name	I/O type	Description	GPIO pin multiplexing
IND_RST_WL	I	Independent software reset for Wi-Fi	GPIO[10]
IND_RST_NB	I	Independent software reset for Bluetooth LE/802.15.4 radio	GPIO[11]

Table 17: Software reset pins

2.6 External coexistence interfaces

External coexistence interfaces enable signaling between the internal radios and external co-located wireless devices for optimal performance when sharing the wireless medium. External radios can be connected to the 5-wire packet traffic arbitration interface (PTA) on MAYA-W4 or the 2-wire wireless coexistence interface 2 (WCI-2). The WCI-2 message format and message type comply with Bluetooth Low Energy special interest group (SIG) core specification volume 7, part C.

Pin name	I/O type	Description	GPIO pin multiplexing
EXT_STATE	I	External radio state input signal (optional) External radio traffic direction (Tx/Rx): 1: Tx 0: Rx	GPIO[22]
EXT_GNT	O	External radio grant output signal (mandatory)	GPIO[20]
EXT_FREQ	I	External radio frequency input signal (optional) Frequency overlap between external radio and Wi-Fi: 1: overlap 0: non-overlap This signal is useful when the external radio is a frequency hopping device.	GPIO[18]
EXT_PRI	I	External radio input priority signal (optional) Priority of the request from the external radio. Can support 1 bit priority (sample once) and 2-bit priority (sample twice). Can also have Tx/Rx information following the priority information if EXT_STATE is not used.	GPIO[21]
EXT_REQ	I	Request from the external radio (mandatory)	GPIO[19]

Table 18: PTA external coexistence interface description

Pin name	I/O type	Description	GPIO pin multiplexing
WCI_IN	I	WCI-2 serial interface input	GPIO[22]
WCI_OUT	O	WCI-2 serial interface output	GPIO[18]

Table 19: WCI external coexistence interface description

2.7 JTAG

The module includes a JTAG test interface that is supported using the GPIO pins.

Pin name	I/O type	Description	GPIO pin multiplexing
JTAG_TCK	I	JTAG test clock input signal	GPIO[2]
JTAG_TMS	I	JTAG controller select input signal	GPIO[3]
JTAG_TDI	I	JTAG test data input signal	GPIO[4]
JTAG_TDO	O	JTAG test data output signal	GPIO[5]

Table 20: JTAG interface description

2.8 GPIOs

MAYA-W4 supports up to 22 GPIO pins, which may be multi-functional pins that can be assigned to different interfaces. On power-up and reset, the GPIO pins assume a high-impedance tristate. After firmware initialization, the GPIO pins are programmed in line with their usual functionality.

For information describing what GPIOs are used for each interface, see UART interface, SPI interface, Wake-up and reset interfaces, External coexistence interfaces, and JTAG. All other GPIOs are described in the Pin definition.

3 Pin definition

3.1 Pin assignment

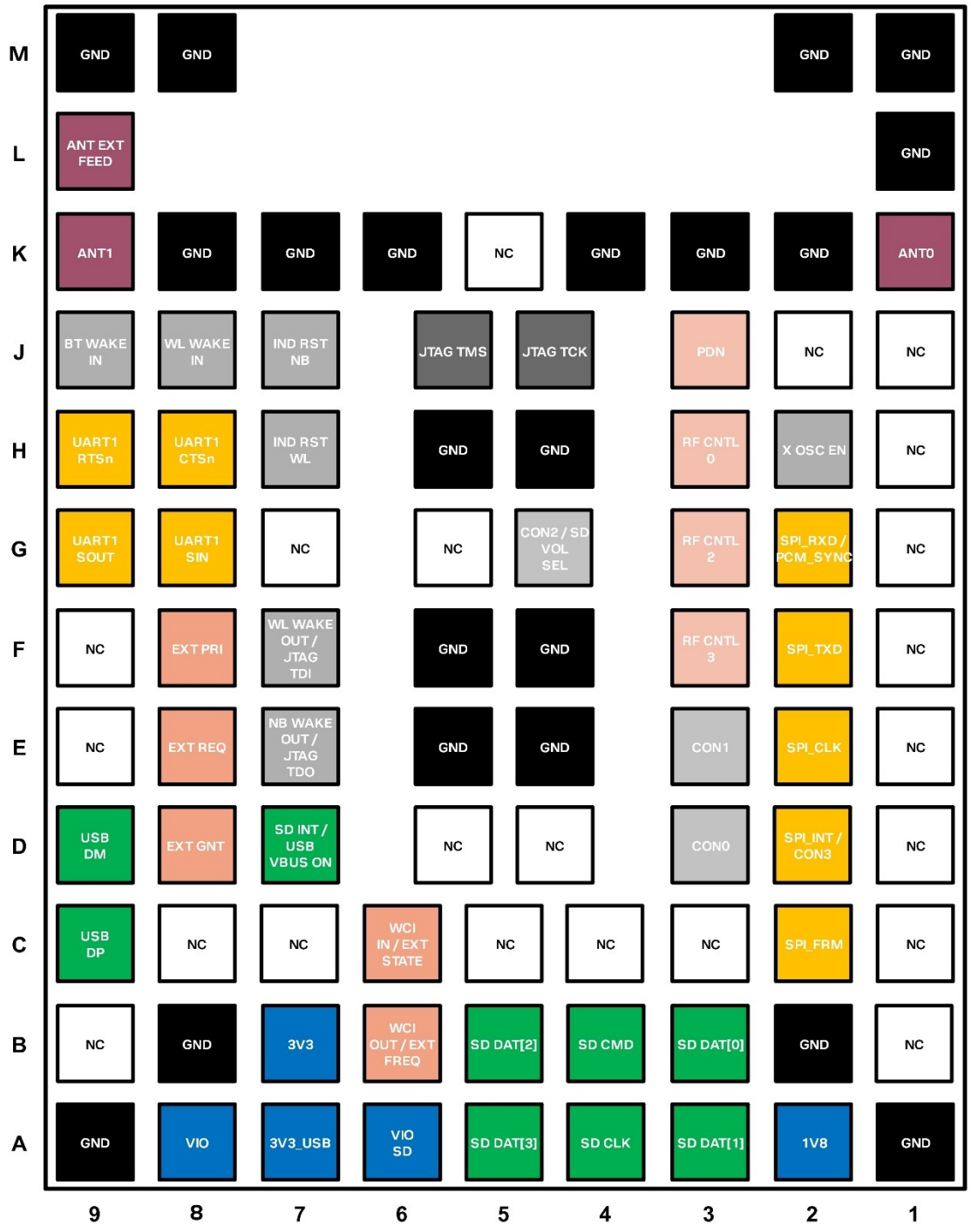


Figure 11: MAYA-W4 series pin assignment (top view)

All signal pins are mounted in a land grid array (LGA) package on the bottom side of the PCB. The RF pins (**RF_ANT0** and **RF_ANT1)** are not available on U.FL connector variants of MAYA-W4.

No.	Name	Pin type[1]	Chipset pin	Description	Power-down state	Power supply domain
A1	GND	GND		Ground	-	
A2	1V8	PWR		1.8 V supply	-	1V8
A3	SD_DAT[1]	I/O	SD_DAT[1]	SDIO data 1	Tristate	VIO_SD
A4	SD_CLK	I	SD_CLK	SDIO clock	Tristate	VIO_SD
A5	SD_DAT[3]	I/O	SD_DAT[3]	SDIO data 3	Tristate	VIO_SD
A6	VIO_SD	PWR		1.8 V / 3.3 V SDIO supply	-	VIO_SD
A7	3V3_USB	PWR		3.3 V USB interface supply. Do not connect when SDIO is used.	-	3V3_USB
A8	VIO	PWR		1.8 V / 3.3 V I/O supply	-	VIO
A9	GND	GND		Ground	-	
B1	NC	NC		Reserved	-	
B2	GND	GND		Ground	-	
B3	SD_DAT[0]	I/O	SD_DAT[0]	SDIO data 0	Tristate	VIO_SD
B4	SD_CMD	I/O	SD_CMD	SDIO command/response	Tristate	VIO_SD
B5	SD_DAT[2]	I/O	SD_DAT[2]	SDIO data 2	Tristate	VIO_SD
B6	WCI_OUT	I/O	GPIO[18] / WCI-2_SOUT/ EXT_FREQ	Multi-functional pin: • GPIO[18] • WCI-2 coexistence serial interface output • PTA mode: EXT_FREQ – External radio frequency signal (input)	Tristate	VIO
B7	3V3	PWR		3.3 V supply	-	3V3
B8	GND	GND		Ground	-	
B9	NC	NC		Reserved	-	
C1	NC	NC		Reserved	-	
C2	SPI_FRM	I/O	GPIO[8] / SPI_FRM / BLE_HOST_TRIG0	Multi-functional pin: • GPIO[8] • SPI mode: SPI frame signal (input) • Bluetooth LE host trigger pin 0 (input/output)	Tristate	VIO
C4	NC	NC		Reserved	-	
C5	NC	NC		Reserved	-	
C6	WCI_IN	I/O	GPIO[22] / WCI-2_SIN	Multi-functional pin: • GPIO[22] • WCI-2 coexistence serial interface input • PTA mode: EXT_STATE - External radio state signal (input)	Tristate	VIO
C8	NC	NC		Reserved	-	
C9	USB_DP	I/O	USB_DP	USB 2.0 Serial differential plus		3V3
D1	NC	NC		Reserved	-	
D2	SPI_INT / CON[3]	I/O	SPI_INT / CONFIG_ HOST_BOOT[3]	Multi-functional pin: • SPI mode: SPI interrupt signal (output) • Host configuration pin: CON[3]	Tristate	1V8
D3	CON[0]	I	CONFIG_ HOST_BOOT[0]	Host configuration pin: CON[0]	Tristate	1V8
D7	USB_VBUS_ON	I/O	GPIO[1] / SD_INT / USB_VBUS_ON	Multi-functional pin: • GPIO[1]	Tristate	VIO

[1] I/O notations: I=Input, O=Output, I/O=Input or Output, OD=Open Drain, NC=Not Connected, PWR=Power, GND=Ground, RF=Radio i/f

No.	Name	Pin type[1]	Chipset pin	Description	Power-down state	Power supply domain
				• SD_INT: SDIO interrupt signal (output) • USB_VBUS_ON: USB voltage indicator (input)		
D8	EXT_GNT	I/O	GPIO[20] / EXT_GNT	Multi-functional pin: • GPIO[20] • PTA mode: EXT_GNT - External radio grant signal (output)	Tristate	VIO
D9	USB_DM	I/O	USB_DM	USB 2.0 Serial differential minus		3V3
E1	NC	NC		Reserved	-	
E2	SPI_CLK	I/O	GPIO[9] / SPI_CLK	Multi-functional pin: • GPIO[9] • SPI mode: SPI clock signal (input)	Tristate	VIO
E3	CON[1]	I	CONFIG_HOST_BOOT[1]	Host configuration pin: CON[1]	Tristate	1V8
E4	GND	GND		Ground	-	
E5	GND	GND		Ground	-	
E7	NB_WAKE_OUT / JTAG_TDO	I/O	GPIO[5] / NB_WAKE_OUT / JTAG_TDO	Multi-functional pin: • GPIO[5] • Bluetooth LE/802.15.4 to host wake-up signal (output) • JTAG mode: JTAG test data (output)	Tristate	VIO
E8	EXT_REQ	I/O	GPIO[19] / EXT_REQ	Multi-functional pin: • GPIO[19] • PTA mode: EXT_REQ – External radio request signal (input)	Tristate	VIO
E9	NC	NC		Reserved	-	
F1	NC	NC		Reserved	-	
F2	SPI_TXD	I/O	GPIO[6] / SPI_TXD / BLE_HOST_TRIG1	Multi-functional pin: • GPIO[6] • SPI mode: SPI transmit signal (output) • Bluetooth LE host trigger pin 1 (input/output)	Tristate	VIO
F3	RF_CNTL3	O	RF_CNTL3	RF control line 3 (output), used to control an external Wi-Fi antenna diversity switch	Drive high	3V3
F4	GND	GND		Ground	-	
F5	GND	GND		Ground	-	
F7	WL_WAKE_OUT / JTAG_TDI	I/O	GPIO[4] / WL_WAKE_OUT / JTAG_TDI	Multi-functional pin: • GPIO[4] • Wi-Fi radio to host wake-up signal (output) • JTAG mode: JTAG test data (input)	Tristate	VIO
F8	EXT_PRI	I/O	GPIO[21] / EXT_PRI	Multi-functional pin: • GPIO[21] • PTA mode: EXT_PRI – external radio priority signal (input)	Tristate	VIO
F9	NC	NC		Reserved	-	
G1	NC	NC		Reserved	-	
G2	SPI_RXD	I/O	GPIO[7] / SPI_RXD / PCM_SYNC / BLE_HOST_TRIG2	Multi-functional pin: • GPIO[7] • SPI mode: SPI receive signal (input) • Bluetooth LE audio PCM frame sync (input)	Tristate	VIO

No.	Name	Pin type[1]	Chipset pin	Description	Power-down state	Power supply domain
				• Bluetooth LE host trigger pin 2 (input/output)		
G3	RF_CNTL2	O	RF_CNTL2	RF control line 2 (output)	Drive low	3V3
G4	CON[2]	I/O	CONFIG_HOST_BOOT[2] / SD_VOLTAGE_ SEL	Multi-functional pin: • Host configuration pin: CON[2] • SD_VOLTAGE_SEL: SDIO voltage select signal (output)	Tristate	1V8
G5	NC	NC		Reserved	-	
G7	NC	NC		Reserved	-	
G8	UART_SIN	I/O	GPIO[14] / UART_SIN	Multi-functional pin: • GPIO[14] • UART serial input signal	Tristate	VIO
G9	UART_SOUT	I/O	GPIO[15] / UART_SOUT	Multi-functional pin: • GPIO[15] • UART serial output signal	Tristate	VIO
H1	NC	NC		Reserved	-	
H2	XOSC_EN	I/O	GPIO[0] / XOSC_EN	Multi-functional pin: • GPIO[0] • Oscillator enable mode : XOSC_EN	Tristate	VIO
H3	RF_CNTL0	I/O	RF_CNTL0 / CONFIG_XOSC_SEL	RF control line 0 (output) Configuration pin: CON[5]. Must be set to 1.	Drive low	3V3
H4	GND	GND		Ground	-	
H5	GND	GND		Ground	-	
H7	IND_RST_WL	I/O	GPIO[10]/ IND_RST_WL	Multi-functional pin: • GPIO[10] • Independent software reset for Wi-Fi radio (input)	Tristate	VIO
H8	UART_CTS	I/O	GPIO[12]/ UART_CTSn	Multi-functional pin: • GPIO[12] • UART clear-to-send input signal (active low)	Tristate	VIO
H9	UART_RTS	I/O	GPIO[13]/ UART_RTSn	Multi-functional pin: • GPIO[13] • UART request-to-send output signal (active low)	Tristate	VIO
J1	NC	NC		Reserved	-	
J2	NC	NC		Reserved	-	
J3	PDn	I	PDn	Power-down signal (input) 0 – power-down mode 1 – normal mode This pin has an always-on internal 51 kΩ pull-up on the module. It can accept an input of 1.75 – 3.63 V.	-	3V3
J4	JTAG_TCK	I/O	GPIO[2]/ JTAG_TCK	Multi-functional pin : • GPIO[2] • JTAG mode: JTAG test clock (input)	Tristate	VIO
J5	JTAG_TMS	I/O	GPIO[3]/ JTAG_TMS	Multi-functional pin: • GPIO[3] • JTAG mode: JTAG test mode select (input)	Tristate	VIO
J7	IND_RST_NB	I/O	GPIO[11]/	Multi-functional pin:	Tristate	VIO

No.	Name	Pin type[1]	Chipset pin	Description	Power-down state	Power supply domain
			IND_RST_NB	• GPIO[11] • Independent software reset for Bluetooth LE/802.15.4 radio (input)		
J8	WL_WAKE_IN	I/O	GPIO[16]/ WL_WAKE_IN	Multi-functional pin: • GPIO[16] • Wi-Fi radio wake-up signal (input)	Tristate	VIO
J9	NB_WAKE_IN	I/O	GPIO[17]/ NB_WAKE_IN	Multi-functional pin: • GPIO[17] • Bluetooth LE/802.15.4 radio wake-up signal (input)	Tristate	VIO
K1	RF_ANT0	RF		Antenna pin for Wi-Fi I/O. See Table 14.	-	1V8
K2	GND	GND		Ground	-	
K3	GND	GND		Ground	-	
K4	GND	GND		Ground	-	
K5	NC	NC		Reserved	-	
K6	GND	GND		Ground	-	
K7	GND	GND		Ground	-	
K8	GND	GND		Ground	-	
K9	RF_ANT1	RF		Antenna pin for Bluetooth Low Energy/802.15.4 or combined Bluetooth Low Energy/802.15.4 and Wi-Fi I/O. See Table 14.	-	1V8
L1	GND	GND		Ground	-	
L9	ANT_FEED	RF		External antenna feed pin for module variants with an internal PCB antenna. Others: NC See Table 14.	-	
M1	GND	GND		Ground	-	
M2	GND	GND		Ground	-	
M8	GND	GND		Ground	-	
M9	GND	GND		Ground	-	

Table 21: MAYA-W4 series pin description

4 Electrical specifications

⚠ Stressing the device above one or more of the ratings of the Absolute maximum ratings can cause permanent damage. These are stress ratings only. Operating the module at these ratings or in conditions other than those specified in the Operating conditions should be avoided. Exposure to absolute maximum rating conditions for extended periods can affect device reliability.

☞ All given application information is only advisory and does not form part of the specification.

4.1 Absolute maximum ratings

Symbol	Description	Min.	Max.	Units
3V3	Power supply voltage	-	3.96	V
1V8	Power supply voltage 1.8 V	-	2.16	V
VIO	I/O supply voltage 1.8 V	-	2.16	V
	I/O supply voltage 3.3 V	-	3.96	V
VIO_SD	SDIO power supply voltage 1.8 V	-	2.16	V
	SDIO power supply voltage 3.3 V	-	3.96	V
$T_{STORAGE}$	Storage temperature	-45	+85	°C

Table 22: Absolute maximum ratings

⚠ The product is not protected against overvoltage or reversed voltages. If necessary, voltage spikes exceeding the power supply voltage specifications given in Table 22 must be limited to values within the specified boundaries by using appropriate protection devices.

4.1.1 Maximum ESD ratings

Applicability	Min.	Max.	Units
Human Body Model (HBM), ANSA/ESDA/JEDEC JS-001-2014.	-2000	+2000	V
Charged Device Model (CDM), JESD22-C101.	-500	+500	V

Table 23: Maximum ESD ratings

4.2 Recommended operating conditions

Symbol	Parameter	Min.	Typ	Max.	Units
3V3	Power supply voltage 3.3 V	3.14	3.3	3.46	V
1V8	Power supply voltage 1.8 V	1.71	1.80	1.89	V
VIO	I/O supply voltage 1.8 V	1.71	1.80	1.89	V
	I/O supply voltage 3.3 V	3.14	3.30	3.46	V
VIO_SD	SDIO supply voltage 1.8 V	1.71	1.80	1.89	V
	SDIO supply voltage 3.3 V	3.14	3.30	3.46	V
T_A	Ambient operating temperature for professional grade modules	-40		+85	°C
T_J	Maximum junction temperature	-	-	125	°C

Table 24: Operating conditions

4.3 Digital pad settings

Symbol	Parameter	VIO	Min.	Max.	Units
V_{IH}	Input high voltage	1.8 V / 3.3 V	0.7*VIO	VIO+0.4	V
V_{IL}	Input low voltage	1.8 V / 3.3 V	-0.4	0.3*VIO	V
V_{HYS}	Input hysteresis	1.8 V / 3.3 V	100	-	mV
V_{OH}	Output high voltage	1.8 V / 3.3 V	VIO-0.4	-	V
V_{OL}	Output low voltage	1.8 V / 3.3 V	-	0.4	V

Table 25: DC characteristics VIO

4.4 Power consumption

4.4.1 Wi-Fi power consumption

Unless otherwise stated, all specifications are valid at 25° C, nominal voltage, and with typical SDIO clock speed of 200 MHz.

Wi-Fi operation modes	3V3 (3.3V) [mA]	1V8 (1.8 V) [mA]	VIO+VIO_SD (1.8 V) [mA]
Power – save modes			
Power down	TBD	TBD	TBD
Wi-Fi only enabled in deep-sleep	TBD	TBD	TBD
Wi-Fi, Bluetooth Low Energy and 802.15.4 in deep-sleep mode	TBD	TBD	TBD
IEEE Power Save DTIM 10 and Bluetooth Low Energy deep-sleep, 2G	TBD	TBD	TBD
IEEE Power Save DTIM 5 and Bluetooth Low Energy deep-sleep, 2G	TBD	TBD	TBD
IEEE Power Save DTIM 3 and Bluetooth Low Energy deep-sleep, 2G	TBD	TBD	TBD
IEEE Power Save DTIM 1 and Bluetooth Low Energy deep-sleep, 2G	TBD	TBD	TBD
IEEE Power Save DTIM 10 and Bluetooth Low Energy deep-sleep, 5G	TBD	TBD	TBD
IEEE Power Save DTIM 5 and Bluetooth Low Energy deep-sleep, 5G	TBD	TBD	TBD
IEEE Power Save DTIM 3 and Bluetooth Low Energy deep-sleep, 5G	TBD	TBD	TBD
IEEE Power Save DTIM 1 and Bluetooth Low Energy deep-sleep, 5G	TBD	TBD	TBD
Active transmit modes for 2G Wi-Fi operation [1]			
DSSS 1 Mbit/s, BW20, Ch6, 18 dBm	216	84	TBD
CCK 11 Mbit/s, BW20, Ch6, 18 dBm	219	83	TBD
OFDM 6 Mbit/s, BW20, Ch6, 18dBm	216	97	TBD
OFDM 54 Mbit/s, BW20, Ch6, 18dBm	221	97	TBD
11n, MCS0, HT20, Ch6, 17 dBm	199	96	TBD
11n, MCS7, HT20, Ch6, 17 dBm	204	96	TBD
11ax, MCS0, HE20, Ch6, 20 dBm	176	95	TBD
11ax, MCS9, HE20, Ch6, 20 dBm	178	94	TBD
Active transmit modes for 5G Wi-Fi operation [1]			
OFDM 6 Mbit/s, BW20, Ch100, 17 dBm	299	174	TBD
OFDM 54 Mbit/s, BW20, Ch100, 17 dBm	305	173	TBD
11n, MCS0, HT20, Ch100, 16 dBm	279	173	TBD
11n, MCS7, HT20, Ch100, 16 dBm	284	171	TBD
11ac, MCS0, VHT20, Ch100, 16 dBm	278	173	TBD
11ac, MCS8, VHT20, Ch100, 16 dBm	286	171	TBD
11ax, MCS0, HE20, Ch100, 15 dBm	262	172	TBD
11ax, MCS9, HE20, Ch100, 15 dBm	267	169	TBD

Wi-Fi operation modes	3V3 (3.3V) [mA]	1V8 (1.8 V) [mA]	VIO+VIO_SD (1.8 V) [mA]
Receive modes for 2G Wi-Fi operation [1]			
CCK 11 Mbit/s, BW20, Ch6, -50 dBm	TBD	TBD	TBD
OFDM 54 Mbit/s, BW20, Ch6, -50 dBm	TBD	TBD	TBD
MCS7, HT20, Ch6, -50 dBm	TBD	TBD	TBD
MCS11, HE20, Ch6, -50 dBm	TBD	TBD	TBD
Receive modes for 5G Wi-Fi operation [1]			
OFDM 54, BW20, Ch100, -50dBm	TBD	TBD	TBD
MCS7, HT20, Ch100, -50 dBm	TBD	TBD	TBD
MCS8, VHT20, Ch100, -50 dBm	TBD	TBD	TBD
MCS11, HE20, Ch100, -50 dBm	TBD	TBD	TBD
Peak current (at room temperature)			
Active transmission	TBD	TBD	TBD
Firmware initialization	TBD	TBD	TBD

Table 26: Typical Wi-Fi radio current consumption with different modes of operation

4.4.2 Bluetooth Low Energy power consumption

☞ Unless otherwise stated, all specifications are valid at 25° C and given at nominal voltage.

Bluetooth Low Energy operation modes	3V3 (3.3 V) [mA]	1V8 (1.8 V) [mA]	VIO+VIO_SD (1.8 V) [mA]
Operating modes			
Bluetooth Low Energy and 802.15.4 only in deep sleep	TBD	TBD	TBD
Bluetooth Low Energy in idle (without deep sleep)	TBD	TBD	TBD
Bluetooth Low Energy classic inquiry scan	TBD	TBD	TBD
Bluetooth Low Energy classic page scan	TBD	TBD	TBD
Bluetooth Low Energy LE advertisement (interval = 1.28 s)	TBD	TBD	TBD
Bluetooth Low Energy LE scanning (interval = 1.28 s, window = 11.25 ms)	TBD	TBD	TBD
BLE, 2 Mbit/s, Ch 0, 13 dBm	34	89	TBD
BLE, 2 Mbit/s, Ch39, 13 dBm	34	90	TBD
BLE, 1 Mbit/s, Ch 0, 13 dBm	33	102	TBD
BLE, 1 Mbit/s, Ch39, 13 dBm	31	103	TBD
BLE, 0.5 Mbit/s, Ch 0, 13 dBm	33	94	TBD
BLE, 0.5 Mbit/s, Ch39, 13 dBm	34	92	TBD
BLE, 0.125 Mbit/s, Ch 0, 13 dBm	34	110	TBD
BLE, 0.125 Mbit/s, Ch39, 13 dBm	32	103	TBD
Active receive mode [1]			
Bluetooth Low Energy Low Energy, 1 Mbit/s	TBD	TBD	TBD
Bluetooth Low Energy Low Energy, 2 Mbit/s	TBD	TBD	TBD

Table 27: Typical Bluetooth Low Energy current consumption with different modes of operation

4.4.3 802.15.4 power consumption

☞ Unless otherwise stated, all specifications are valid at 25° C and given at nominal voltage.

802.15.4 operation modes	3V3 (3.3 V) [mA]	1V8 (1.8 V) [mA]	VIO+VIO_SD (1.8 V) [mA]
Operating modes			
802.15.4 transmit, Ch11, 13 dBm	31	101	TBD
802.15.4 transmit, Ch20, 13 dBm	28	102	TBD
Active receive mode			
802.15.4 peak receive idle mode	TBD	TBD	TBD
802.15.4 peak receive active mode	TBD	TBD	TBD

Table 28: Typical 802.15.4 current consumption

4.5 Radio specification

4.5.1 Bluetooth Low Energy

Parameter	Specification (typical values)
RF Frequency Range	2.402 – 2.480 GHz
Supported Modes	Bluetooth Low Energy 5.4 (LE) • LE long range coded PHY • LE 2 Mbit/s PHY
Transmit Power [1] [2][3]	Bluetooth LE 1M: 14 dBm Bluetooth LE 2M: 9 dBm Bluetooth LE Coded: 14 dBm
Receiver Sensitivity	Bluetooth LE Coded 125 kb/s: -105 dBm Bluetooth LE Coded 500 kb/s: -98 dBm Bluetooth LE 1M: -96 dBm Bluetooth LE 2M: -94 dBm

Table 29: Bluetooth Low Energy radio parameters

[1] Values are valid at antenna pin ports and at room temperature.
[2] Single antenna variants typically have output power values up to 2 dB lower.
[3] Bluetooth Low Energy transmit power must be limited to <= 10 dBm EIRP to comply with EN 300 328 regulations.

4.5.2 IEEE 802.15.4

Parameter	Specification (typical Values)
RF Frequency Range	2.405 – 2.480 GHz
Supported Mode	IEEE 802.15.4-2020 • Support for Thread in 2.4 GHz band • Support for Matter over Thread
Modulation	O-QPSK
Transmit Power [1] [2]	Transmit Power up to 14 dBm
Receiver sensitivity [1] [2]	Typical receiver sensitivity is -105 dBm

Table 30: IEEE 802.15.4 parameters

[1] Values are valid at antenna pin ports and at room temperature.
[2] Single antenna variants typically have power output values up to 1 dB lower.

4.5.3 Wi-Fi

MAYA-W4 series modules support dual-band Wi-Fi with 802.11a/b/g/n/ac/ax operation in the 2.4 GHz and 5 GHz radio bands. The module is designed to operate in only one frequency band at a time.

Parameter	Operation Mode	Specification
RF Frequency range	802.11b/g/n/ax	2.400 – 2.4835 GHz
	802.11a/n/ac/ax	4.900 – 5.895 GHz
Modulation	802.11b	CCK and DSSS
	802.11a/g/n/ac/ax	OFDM
Supported data rates	802.11b	1, 2, 5.5, 11 Mbit/s
	802.11a/g	6, 9, 12, 18, 24, 36, 48, 54 Mbit/s
	802.11n	MCS0 – MCS7
	802.11 ac	MCS0 – MCS8
	802.11 ax	MCS0 – MCS9
Supported channel bandwidth	802.11b/g/a/n/ac/ax	20 MHz
Supported guard interval (GI)	802.11ax	800, 1600, 3200 ns

Table 31: Wi-Fi radio parameters

Parameter		Operation mode	802.11 EVM limit	Specification (typical output power tolerance ±2 dB) [1]	
				Dual Antenna Variants	Single antenna Variants
Maximum transmit power	2.4 GHz	DSSS/CCK	-9 dB	TBD dBm	18 dBm
		OFDM, BPSK	-5 dB	TBD dBm	15 dBm
		OFDM, QPSK	-13 dB	TBD dBm	15 dBm
		OFDM, 16-QAM	-19 dB	TBD dBm	15 dBm
		OFDM, 64-QAM, 3/4	-25 dB	TBD dBm	15 dBm
		OFDM, 64-QAM, 5/6	-27 dB	TBD dBm	15 dBm
		OFDM, 256-QAM, 3/4	-35 dB	TBD dBm	15 dBm
		OFDM, 256-QAM, 5/6	-35 dB	TBD dBm	15 dBm
	5 GHz	OFDM, BPSK	-5 dB	TBD dBm	15 dBm
		OFDM, QPSK	-13 dB	TBD dBm	15 dBm
		OFDM, 16-QAM	-19 dB	TBD dBm	15 dBm
		OFDM, 64-QAM, 3/4	-25 dB	TBD dBm	15 dBm
		OFDM, 64-QAM, 5/6	-27 dB	TBD dBm	15 dBm
		OFDM, 256-QAM, 3/4	-30 dB	TBD dBm	15 dBm
		OFDM, 256-QAM, 5/6	-32 dB	TBD dBm	15 dBm

Table 32: Target Wi-Fi radio maximum transmit power parameters

Band	Operating mode	Data rate	Specification (typical values tolerance ±2 dBm) [1]
2.4 GHz	802.11b	1 Mbit/s / 2 Mbit/s	-96 dBm / -95 dBm
		5.5 Mbit/s / 11 Mbit/s	-94 dBm / -90 dBm
	802.11g	6 Mbit/s / 9 Mbit/s	-93 dBm / -92 dBm
		12 Mbit/s / 18 Mbit/s	-91 dBm / -88 dBm
		24 Mbit/s / 36 Mbit/s	-87 dBm / -83 dBm
		48 Mbit/s / 54 Mbit/s	-79 dBm / -76 dBm
	802.11n	MCS0 / MCS1	-93 dBm / -91 dBm
		MCS2 / MCS3	-89 dBm / -86 dBm
		MCS4 / MCS5	-82 dBm / -78 dBm
		MCS6 / MCS7	-77 dBm / -75 dBm
	802.11ax	MCS0 / MCS1	-93 dBm / -91 dBm
		MCS2 / MCS3	-89 dBm / -87 dBm
		MCS4 / MCS5	-83 dBm / -79 dBm
		MCS6 / MCS7	-77 dBm / -76 dBm
		MCS8 / MCS9	-71 dBm / -69 dBm
5 GHz	802.11a	6 Mbit/s / 9 Mbit/s	-91 dBm / -90 dBm
		12 Mbit/s / 18 Mbit/s	-89 dBm / -87 dBm
		24 Mbit/s / 36 Mbit/s	-84 dBm / -80 dBm
		48 Mbit/s / 54 Mbit/s	-76 dBm / -75 dBm
	802.11n	MCS0 / MCS1	-90 dBm / -88 dBm
		MCS2 / MCS3	-86 dBm / -83 dBm
		MCS4 / MCS5	-80 dBm / -76 dBm
		MCS6 / MCS7	-74 dBm / -73 dBm
	802.11ac	MCS0 / MCS1	-90 dBm / -88 dBm
		MCS2 / MCS3	-87 dBm / -84 dBm
		MCS4 / MCS5	-80 dBm / -76 dBm
		MCS6 / MCS7	-75 dBm / -73 dBm
		MCS8	-69 dBm
	802.11ax	MCS0 / MCS1	-90 dBm / -88 dBm
		MCS2 / MCS3	-84 dBm / -80 dBm
		MCS4 / MCS5	-79 dBm / -75 dBm
		MCS6 / MCS7	-71 dBm / -70 dBm
		MCS8 / MCS9	-65 dBm / -63 dBm

Table 33: Target Wi-Fi receiver characteristics

[1] Values are valid at antenna pin ports and at room temperature.

4.5.4 Antenna radiation patterns

The radiation patterns displayed in Table 34 and Table 35 show the radiation patterns for MAYA-W4 modules with internal (embedded niche) antenna in the middle of each frequency band. Table 36 shows the total radiated power (TRP) and peak gain for the low, mid, and high channel of the 2.4 GHz and 5 GHz frequency bands.

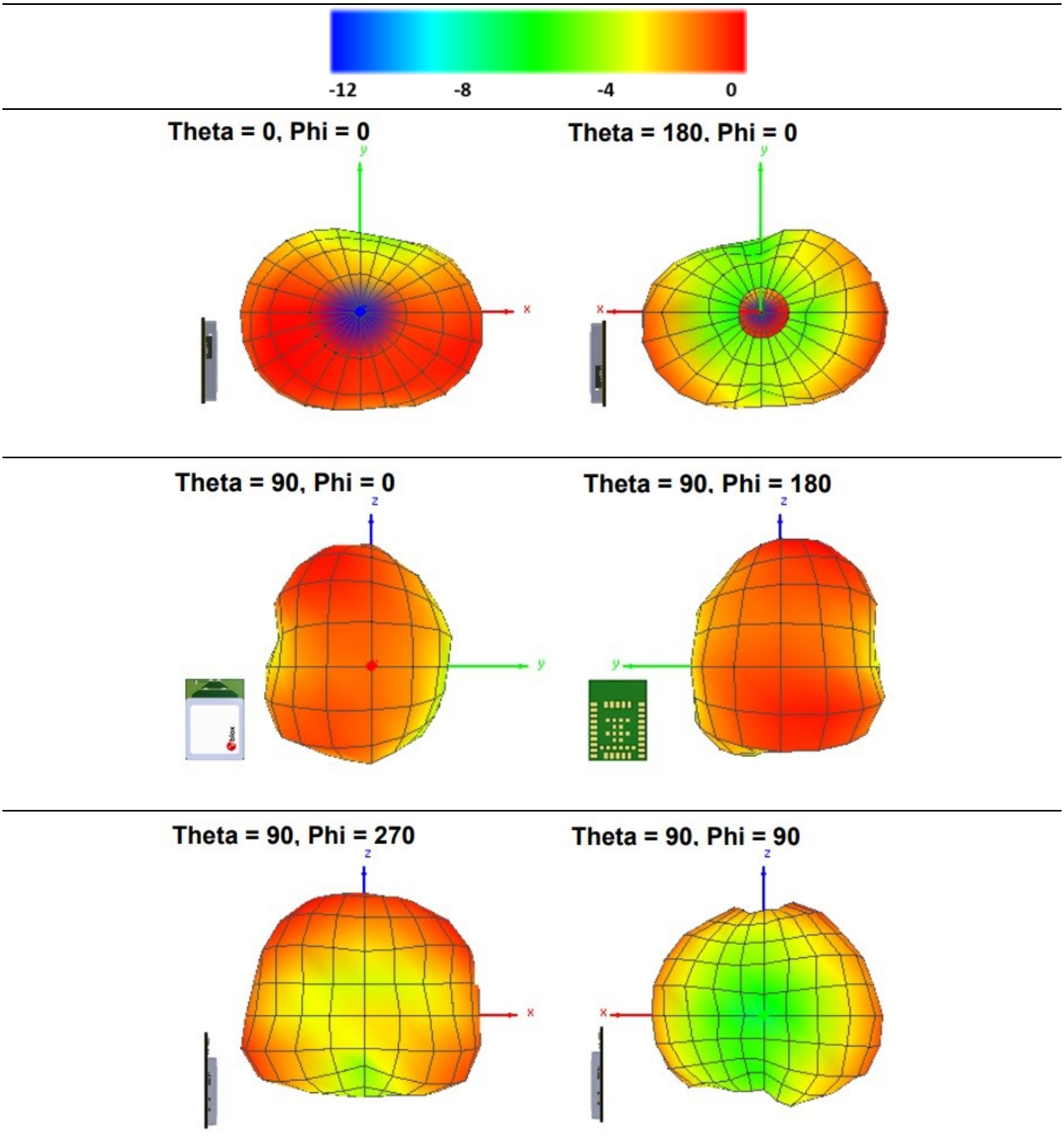
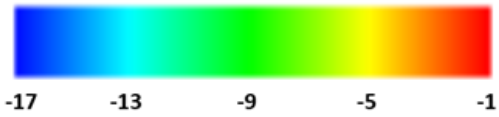
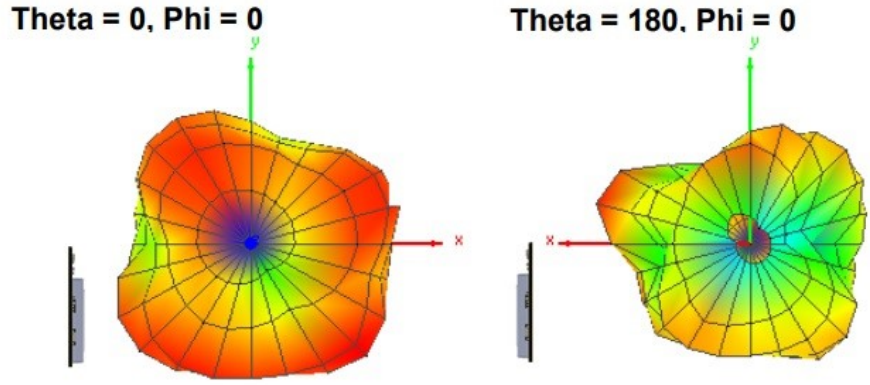
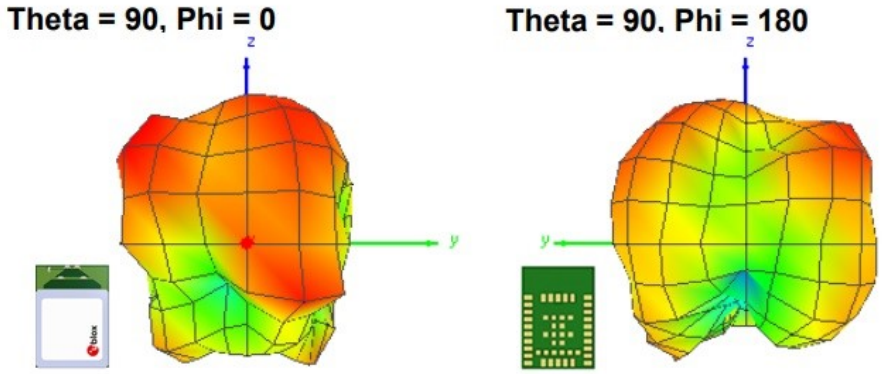


Table 34: Wi-Fi, Bluetooth Low Energy, and 802.15.4 antenna characteristics at 2.437 GHz







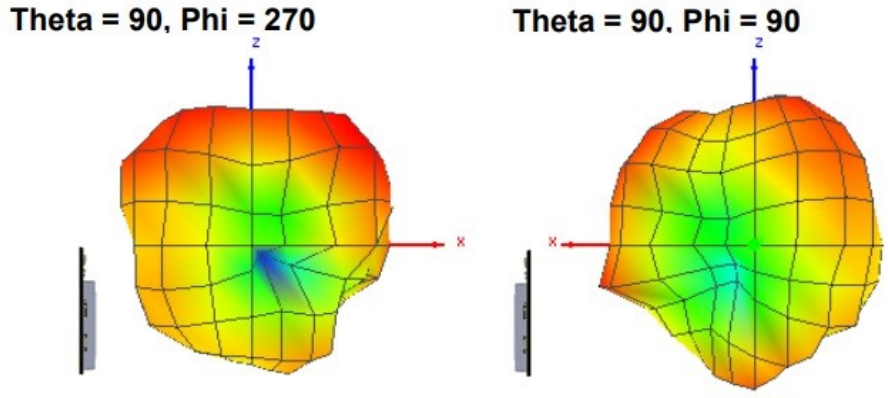


Table 35: Wi-Fi antenna characteristics at 5.50 GHz

Transmission	Measured TRP	Measured peak gain
Channel 1, 2.412 GHz	-4.31 dBm	-0.52 dBi
Channel 6, 2.437 GHz	-4.03 dBm	+0.40 dBi
Channel 13, 2.472 GHz	-3.0 dBm	+1.56 dBi
Channel 36, 5.180 GHz	-4.83 dBm	-1.74 dBi
Channel 100, 5.500 GHz	-1.32 dBm	+1.56 dBi
Channel 159, 5.795 GHz	+1.38 dBm	-2.23 dBi
Channel 177, 5.885 GHz	-4.46 dBm	-0.95 dBi

Table 36: Measured total radiated power and peak gain for 0 dBm transmission power

5 Software support

MAYA-W4 series modules are based on the NXP IW610x chipset family and the drivers and firmware required to operate the modules are developed by NXP. A firmware binary is downloaded to the module by the host operating system driver at start-up.

The following software options are available for the MAYA-W4 module:

- Open-source Linux/Android driver (`mxm_mwifiex`) for mainstream use is available free of charge and already integrated into Linux BSP for NXP i.MX application processors
- MCUXpresso Wi-Fi/Bluetooth Low Energy support for supported NXP MCUs

The software packages typically include:

- Dedicated kernel driver that binds the Wi-Fi device to the kernel. Driver sources are provided.
- Dedicated Wi-Fi firmware image that is uploaded during initialization of the Wi-Fi device.
- Dedicated Bluetooth Low Energy firmware image that is uploaded during initialization of the Bluetooth Low Energy device.
- Wi-Fi and Bluetooth Low Energy release notes and a list of supported software features.
- Laboratory and manufacturing tools.

6 Mechanical specifications

6.1 MAYA-W4 footprint dimensions

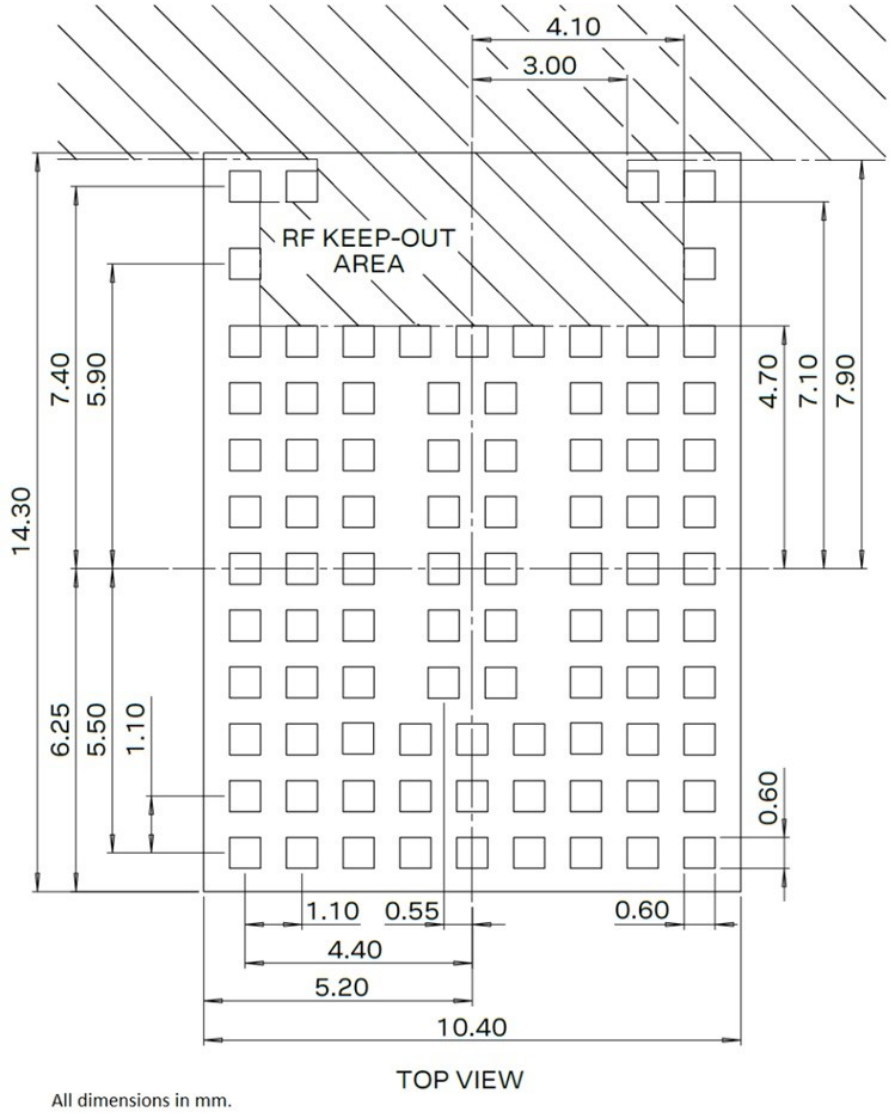


Figure 12: MAYA-W4 footprint

Parameter	Typical	Tolerance
Seating Plane Coplanarity [mm]	<0.1	
Pin Width [mm]	0.60	+0.015/-0.015
Pin Length [mm]	0.60	+0.015/-0.015

Table 37: Dimensions parameters

6.2 MAYA-W4 mechanical specifications

6.2.1 Single pin, dual pin, and internal antenna variants

Figure 13 and Figure 14 show the top and side views of MAYA-W4 single pin, dual pin, and internal antenna module variants. All dimensions are shown in millimeters (mm).

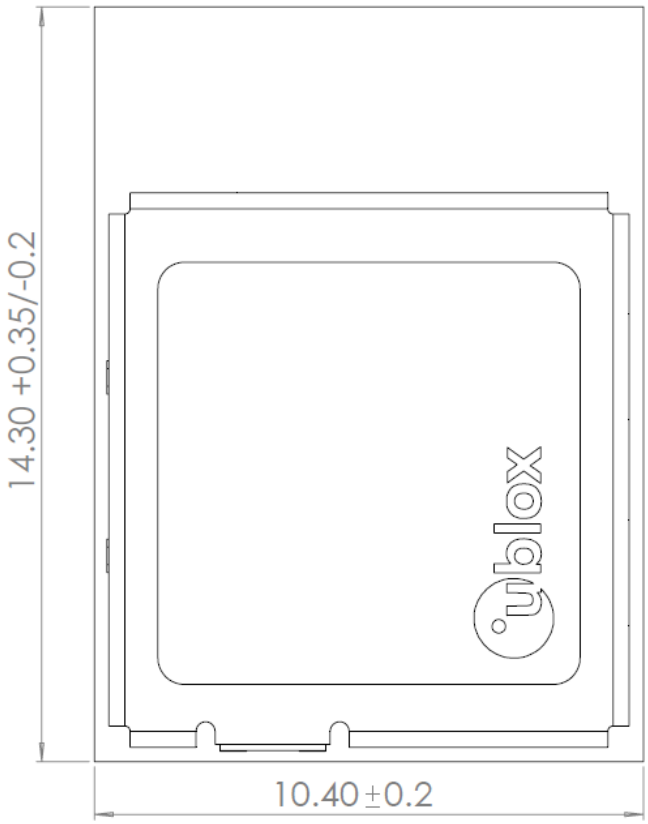


Figure 13: Single pin, dual pin, and internal antenna variants - mechanical specifications (top view)

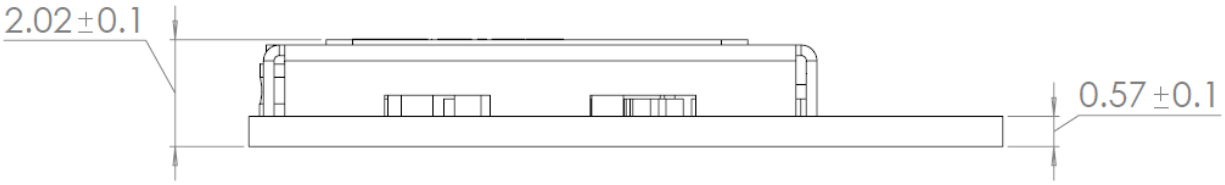


Figure 14: Single pin, dual pin, and internal antenna variants - mechanical specifications (side view)

6.2.2 Single U.FL connector variants

Figure 15 and Figure 16 show the top and side views of MAYA-W4 single U.FL connector variants. All dimensions are shown in millimeters (mm).

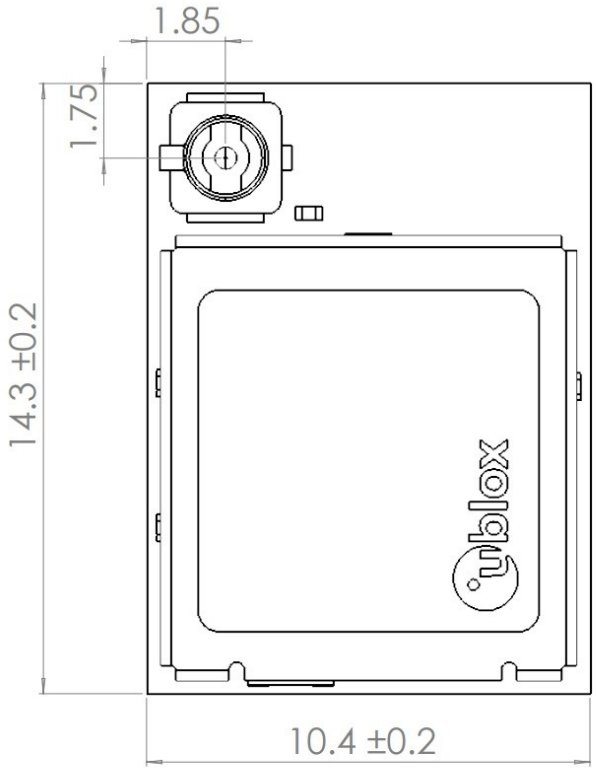


Figure 15: Single U.FL connector variants - mechanical specifications (top view)

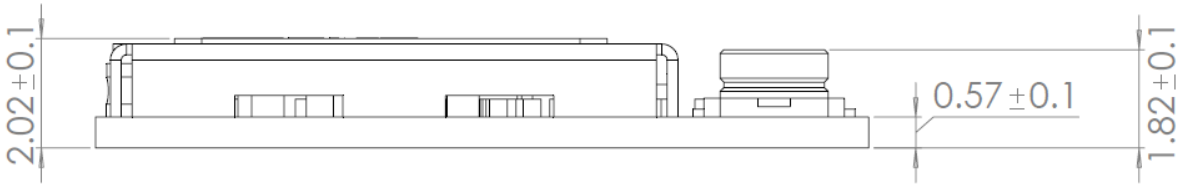


Figure 16: Single UFL connector variants - mechanical specifications (side view)

6.3 Module weight

Module	Typ	Unit
MAYA-W471	<1	g
MAYA-W442, MAYA-W472	<1	g
MAYA-W433, MAYA-W463, MAYA-W473	<1	g
MAYA-W436, MAYA-W466, MAYA-W476	<1	g

Table 38: Module weight

7 Qualifications and approvals

The MAYA-W4 module series is certified for use in the countries/regions shown in Table 39. Other country certifications can be scheduled on request.

Country/region	MAYA-W433	MAYA-W436	MAYA-W442	MAYA-W463	MAYA-W466	MAYA-W471	MAYA-W472	MAYA-W473	MAYA-W476
Europe (RED)	Approved	Approved	Planned	Approved	Approved	Planned	Planned	Approved	Approved
Great Britain (UKCA)	Approved	Approved	Planned	Approved	Approved	Planned	Planned	Approved	Approved
USA (FCC)	Approved	Approved	Planned	Approved	Approved	Planned	Planned	Approved	Approved
Canada (ISED)	Approved	Approved	Planned	Approved	Approved	Planned	Planned	Approved	Approved
Japan (Giteki)	Planned	Planned	Planned	Planned	Planned	Planned	Planned	Planned	Planned

Table 39: Certification

☞ For detailed information about the regulatory requirements that must be met when using MAYA-W4 modules in an end product, see the MAYA-W4 system integration manual [2].

7.1 Bluetooth qualification

End products must be qualified and listed with the Bluetooth Special Interest Group (SIG).

Product declarations are submitted through the Bluetooth SIG Qualification Workspace.

MAYA-W4 series modules are qualified as a Core-Controller configuration in accordance with the Bluetooth Core 5.4 specification.

To list your product that integrates MAYA-W4 with no additional testing required, combine the DN for the Bluetooth stack implemented in the Core-Host configuration with the DN of the Core-Controller configuration shown in Table 40.

Product name	Product type	DID/DN	Product qualification date
MAYA-W433-00B, MAYA-W436-00B, MAYA-W442-00B, MAYA-W463-00B, MAYA-W466-00B, MAYA-W471-00B, MAYA-W472-00B, MAYA-W473-00B, MAYA-W476-00B	Core-Controller configuration	Q360684	2025-06-03

Table 40: MAYA-W4 series Bluetooth qualified design IDs

8 Product handling

8.1 Packaging

MAYA-W4 series modules are delivered as hermetically sealed, reeled tapes to enable efficient production, production lot set-up and tear-down. For more information about packaging, see the Product packaging guide [1].

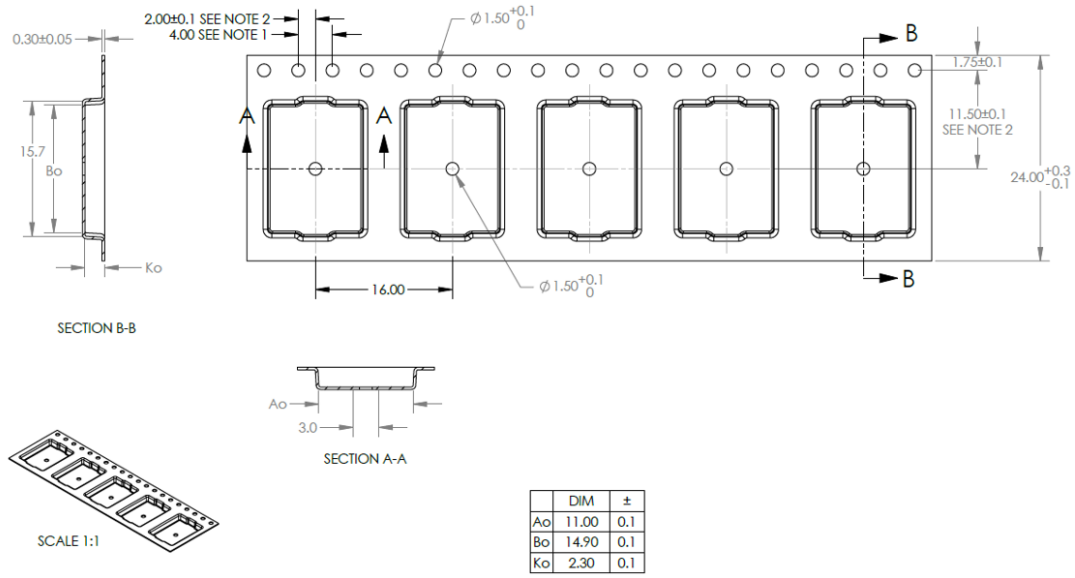
8.1.1 Reels

MAYA-W4 series modules are deliverable in quantities of 500 pieces on a reel. MAYA-W4 series modules are shipped on reel Type A3 as described in the Product packaging guide [1].

8.1.2 Tapes

Figure 17 shows the position and orientation of MAYA-W4 series modules as they are delivered on tape. The dimensions of the tapes are specified in Figure 18.

Figure 17: Orientation of MAYA-W4 modules on tape



	DIM	±
Ao	11.00	0.1
Bo	14.90	0.1
Ko	2.30	0.1

Figure 18: MAYA-W4 tape dimensions

8.2 Moisture sensitivity levels

⚠ MAYA-W4 series modules are rated as MSL Level 4 devices in accordance with the IPC/JEDEC J STD-020 standard. For detailed information, see the moisture sensitive warning label on the MBB (Moisture Barrier Bag).

After opening the dry pack, the modules must be mounted within 72 hours in factory conditions of maximum 30 °C/60%RH or must be stored at less than 10%RH. The modules require baking if the humidity indicator card shows more than 10% when read at 23±5 °C or if the conditions mentioned above are not met. For information about the bake procedure, see also the J-STD-033B standard.

For more information regarding MSL (Moisture Sensitivity Level), labeling, and storage, see also the Packaging information guide [1].

8.3 Reflow soldering

Reflow profiles must be selected in accordance with u-blox recommendations:

- MAYA-W442 and MAYA-W472 are suitable for one-time reflow
- Other MAYA-W4 module variants are suitable for two-time reflow

⚠ Reflow soldering profiles must be selected in accordance with u-blox soldering recommendations described in the system integration manual [2]. Failure to observe these recommendations can result in severe damage to the product.

8.4 ESD handling precautions

⚠ MAYA-W4 series modules are electrostatic sensitive devices (ESD) that demand adherence to special ESD precautions. Failure to observe these recommendations can result in severe damage to the product.

Proper ESD handling and packaging procedures must be applied throughout the processing, handling and operation of any application that incorporates MAYA-W4. We recommend that the module is not handled in a non-ESD protected environment. The RF antenna pins (**RF_ANT0** and **RF_ANT1)** are especially sensitive to ESD, and special care must be taken when connecting antennas. ESD safe soldering equipment is recommended.

9 Labeling and ordering information

9.1 Product labeling

The labels applied to MAYA-W4 series modules include important product information. Figure 19 shows the given label information, where each of the given references are described in Table 41.

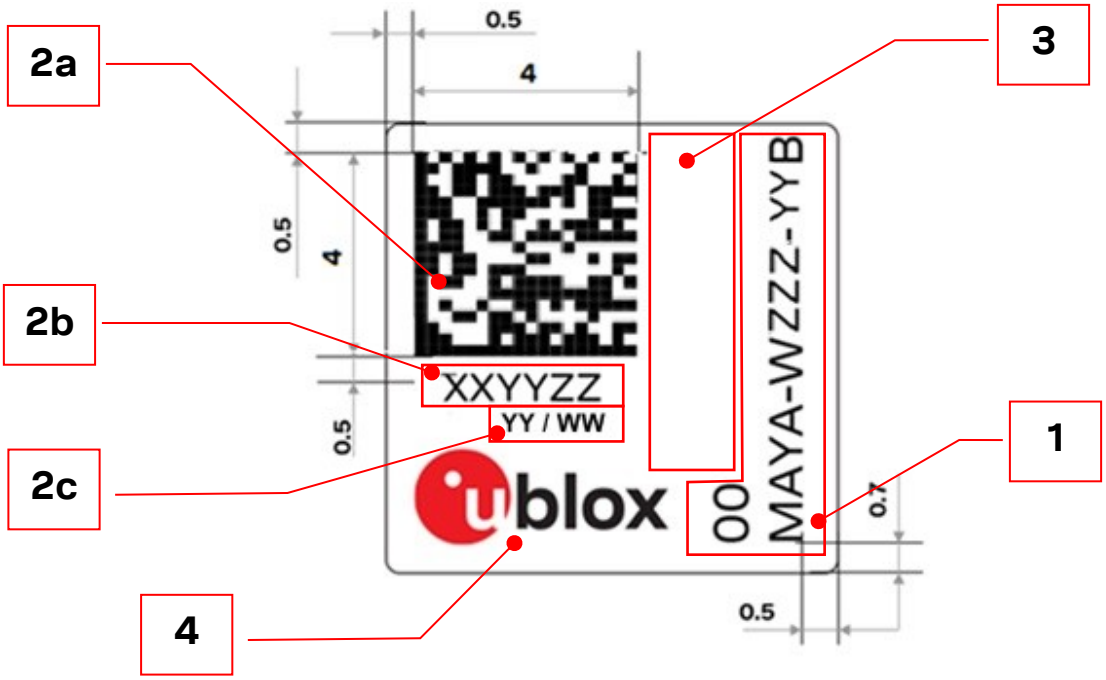


Figure 19: Label information shown on the MAYA-W4 series modules

Reference	Description
1	Text box containing product name (MODEL ID) and version
2a	Data Matrix with unique serial number of 19 alphanumeric symbols: • The first 3 symbols are used for production tracking and are an abbreviated representation of the Type number that is unique to each module variant. • The following 12 symbols represent the unique hexadecimal Bluetooth Low Energy address of the module AABBCCDDEEFF. See also MAC addresses. • The last 4 symbols represent the hardware and firmware version encoded HHFF.
2b	The six last hex symbols of the MAC address (AABBCC**XXYYZZ**)
2c	Date of production in the format YY/WW (year/week)
3	Placeholder for certification IDs
4	u-blox logo, where the red dot indicates the position of pin 1

Table 41: MAYA-W4 series label references

9.2 Explanation of codes

Table 42 describes the three product identifiers, namely the Type number, Model name and Ordering code.

Format	Description	Nomenclature
Model name	Describes the form factor, platform technology and platform variant. Used mostly in product documentation like this data sheet, the model name represents the most common identity for all u-blox products.	PPPP-TGVV
Ordering code	Comprises the model name – with additional identifiers to describe the major product version and quality grade.	PPPP -TGVV-TTQ
Type number	Comprises the model name and ordering code – with additional identifiers that describe minor product versions.	PPPP -TGVV-TTQ-XX

Table 42: Product code formats

9.3 Identification codes

Code	Meaning	Example
PPPP	Form factor	MAYA
TG	Platform (Technology and Generation) T – Dominant technology, For example, W: Wi-Fi, B: Bluetooth Low Energy® G - Generation	W4: Wi-Fi, Generation 4
VV	Variant based on the same platform; range [00…99]	76
TT	Major Product Version	00: first version
Q	Quality grade A: Automotive B: Professional C: Standard	B: Professional grade
XX	Minor product version (not relevant for certification)	Default value: 00

Table 43: Part identification code

9.4 Ordering information

Ordering code	Product
MAYA-W433-00B	MAYA-W433 Single-band Wi-Fi 6 + Bluetooth Low Energy 5.4 module with single antenna pin, 500 pcs/reel, NXP IW610
MAYA-W436-00B	MAYA-W436 Single-band Wi-Fi 6 + Bluetooth Low Energy 5.4 module with single antenna pin and internal PCB antenna, 500 pcs/reel, NXP IW610
MAYA-W442-00B	MAYA-W442 Single-band Wi-Fi 6 + Bluetooth Low Energy 5.4/802.15.4 module with single U. FL connector, 500 pcs/reel, NXP IW610
MAYA-W463-00B	MAYA-W463 Dual-band Wi-Fi 6 + Bluetooth Low Energy 5.4 module with single antenna pin, 500 pcs/reel, NXP IW610
MAYA-W466-00B	MAYA-W466 Dual-band Wi-Fi 6 + Bluetooth Low Energy 5.4 module with single antenna pin and internal PCB antenna, 500 pcs/reel, NXP IW610
MAYA-W471-00B	MAYA-W471 Dual-band Wi-Fi 6 + Bluetooth Low Energy 5.4/802.15.4 module with two antenna pins, 500 pcs/reel, NXP IW610
MAYA-W472-00B	MAYA-W472 Dual-band Wi-Fi 6 + Bluetooth Low Energy 5.4/802.15.4 module with single U. FL connector, 500 pcs/reel, NXP IW610
MAYA-W473-00B	MAYA-W473 Dual-band Wi-Fi 6 + Bluetooth Low Energy 5.4/802.15.4 module with single antenna pin, 500 pcs/reel, NXP IW610
MAYA-W476-00B	MAYA-W476 Dual-band Wi-Fi 6 + Bluetooth Low Energy 5.4/802.15.4 module with single antenna pin and internal PCB antenna, 500 pcs/reel, NXP IW610

Table 44: Product ordering codes

Appendix

A Glossary

Abbreviation	Definition
ADC	Analog to digital converter
BPF	Band pass filter
CAN	Controller area network
CTS	Clear to send
DC	Direct current
DSR	Data set ready
DTR	Data terminal ready
EIRP	Effective isotropic radiated power
GND	Ground
GPIO	General purpose input/output
H	High
I	Input (means that this is an input port of the module)
IEEE	Institute of Electrical and Electronics Engineers
I2C	Inter-integrated circuit
L	Low
LPO	Low power oscillator
MIMO	Multi-input multi-output
MSD	Moisture sensitive device
N/A	Not applicable
O	Output (means that this is an output port of the module)
PCN/IN	Product change notification / Information note
PD	Pull-down
PU	Pull-up
RMII	Reduced media independent interface
RTS	Request to send
RXD	Receive data
SDIO	Secure digital input output
SPI	Serial peripheral interface
TXD	Transmit data
UART	Universal asynchronous Receiver/Transmitter
USB	Universal serial bus

Table 45: Explanation of the abbreviations and terms used

Related documentation

[1] Package information reference guide, UBX-14001652
[2] MAYA-W4 system integration manual, UBXDOC-465451970-3372
[3] MAYA-W4 product summary, UBXDOC-465451970-3565

For product change notifications and regular updates of u-blox documentation, register on our website, www.u-blox.com.

Revision history

Revision	Date	Name	Comments
R01	11-Dec-2024	tngu	Initial release
R02	10-Apr-2025	vbak	Block diagrams updated. Tables 26, 27, 29 updated. Pad tolerance information added (Table 37) Corrected mounting time to 72 hours for MSL 4 in Moisture sensitivity levels. Updated Antenna radiation patterns.
R03	4-Jun-2025	mzes	Added Bluetooth qualification details.

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