

- Rugged carrier board and integrated solution for AGX Thor T5000 / T4000 modules
- Integrated solution contains carrier board, Thor module, embedded Linux OS on M.2 flashdisk, and fan sink thermal solution

- 2x 5GbE
- 2x USB 3.2, 4x USB 2.0
- 3x RS-232/422/485, 1x RS-232
- 4x CAN
- 2x HDMI
- 16x GPIO

- M.2 2280 NVMe
- Minicard
- M.2 E-key
- M.2 B-Key

- 165 x 150mm

- 6.5 x 5.9"

Operating Temp:

- -25 to +80°C



SEGER Carrier Board Block Diagram

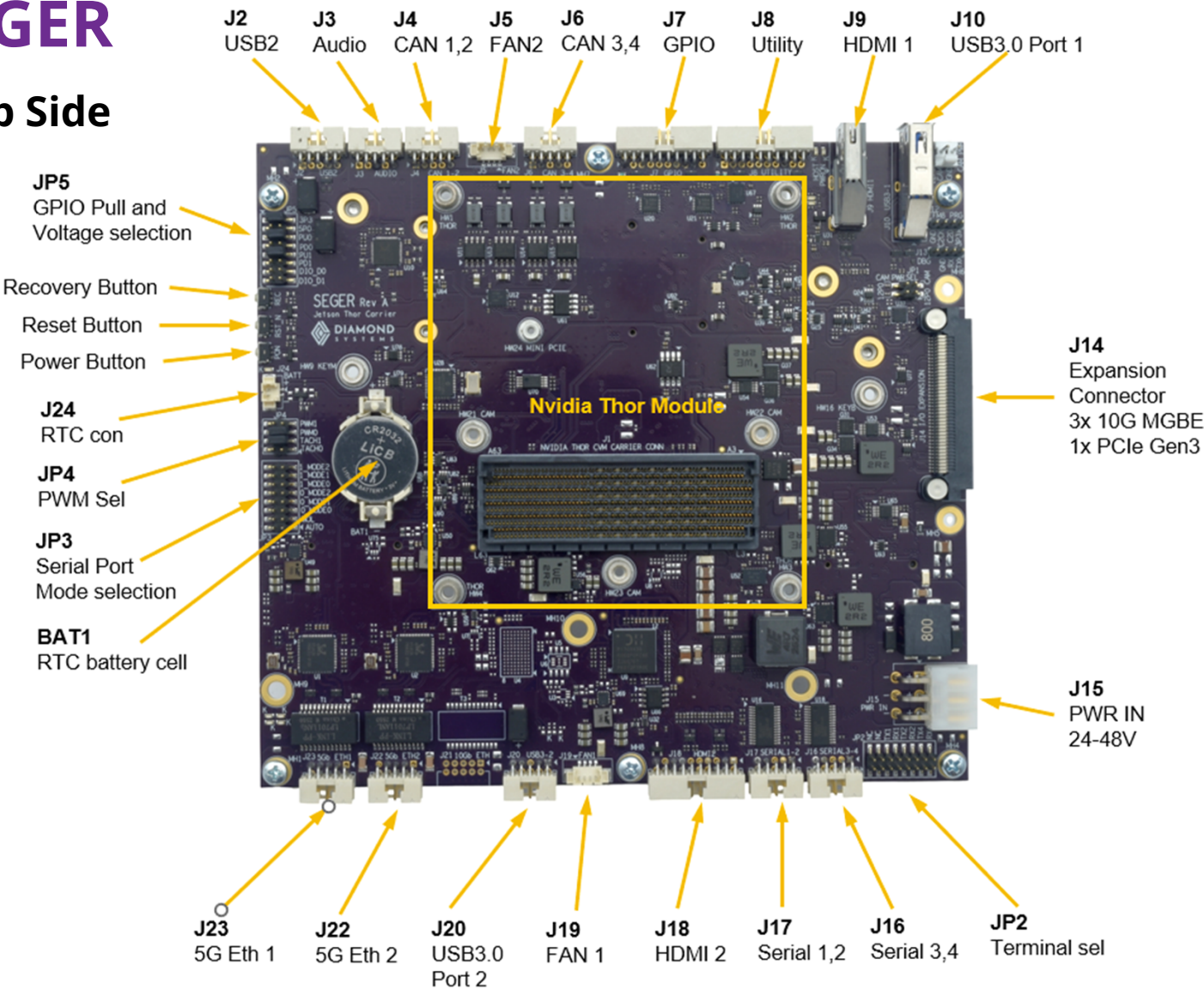
Notes to Block Diagram
U UART **H** USB HUB **P** PCIe

The diagram illustrates the Thor T-5000 Module's architecture, centered around a vertical module spine. Key components include:

- Left Side Interfaces:** M.2 Key M Socket (2242/2280), M.2 Key B Socket (3042/3052), Nano SIM Socket, M.2 Key E Socket (2230), WiFi/BT Control, Mini PCIe Socket 1, I/O expansion Conn., HDMI Vertical Standard Conn., 2x10 RA Latching Conn., Camera Adapter Connector.
- Right Side Interfaces:** Coin Cell Holder, Power Circuits, 1x2 SMT Conn., 2x3 RA Latching Conn., USB2.0 x1, USB2.0 x1, USB3.2 Port 0, USB2.0 Port 1, USB3.2 Port 1, USB2.0 Port 0, PCIe to Eth. Controller (RTL8126), MDI SG Port 1, Magnetics, 2x5 RA Latching Conn., MDI SG Port 2, Magnetics, 2x5 RA Latching Conn., RS-232/422/485 (SP336), RS232/422/485 Port 1, RS232/422/485 Port 2, 2x5 RA Latching Conn., RS-232/422/485 (SP336), RS232/422/485 Port 4, RS232 Port 3, 2x5 RA Latching Conn., Audio Codec (ALC5640), Line In Headphone Out, 2x5 RA Latching Conn., CAN XCVR (ATA6560), CAN Port 1, CAN Port 2, 2x5 RA Latching Conn., CAN XCVR (ATA6560), CAN Port 3, CAN Port 4, 2x5 RA Latching Conn., GPIO Expander1, 8x GPIO, 8x GPIO, GPIO 2x10 RA Latching Conn., EEPROM, GPIO Expander2, 2x GPIO, 2x GPIO, Utility I/O, Level Translator, 1x I2C7, 1x SPI1, 2x PWM, Level Translator, 2x PWM, Fan Conn. 1, Fan Conn. 2, Reset Btn., Power On Btn., Force Rec. Btn.
- Internal Components:** LPDDR5X, QSPI NOR, Thermal Sensor, UPHY Lane[11:8] (PCIe x4, C5, RP), I2C3, UPHY Lane2 (USB 3.2, P2), H2, H3, UPHY Lane0 (USB 3.2, P0) USB1, UPHY Lane1 (USB 3.2, P1) USB0, UPHY Lane4 (PCIe x1 (C2),RP), UART1, UART2, UART3_Debug, I2S3, I2C8, MCLK1, CAN0, CAN1, CAN2, CAN3, UPHY Lane[7:6] (PCIe x2, C3, RP), I2C2, SPI2, UPHY Lane15 (MGBE, C3), UPHY Lane14 (MGBE, C2), UPHY Lane13 (MGBE, C1), UPHY Lane12 (MGBE, C0), DP1_HDMI, DP2_HDMI, DP3_HDMI, DPO_HDMI, CSI[7:0], MCLK[02:03] CAM Control, I2C3, I2C4, I2C5, SPI3, Power Seq. and Reg., PMIC_BBAT, SYS_VIN_HV, SYS_VIN_MV, MUX, I2S1, UPHY Lane3 (PCIe x1, C1, RP), GPIOS, I2C8, USB2, USB3, I2C4, PCIe Switch 1:4 (PI7C9X3G606GP), PCIe x1, PCIe x2, I2C2, SPI2, MGEBE Port 3, MGEBE Port 2, MGEBE Port 1, MDI 10G, 10G Phy AQR113, MGEBE Port 0, N/C, DP1_HDMI, DP2_HDMI, DP3_HDMI, DPO_HDMI, CSI[7:0], MCLK[02:03] CAM Control, I2C3, I2C4, I2C5, SPI3, Reset, Power On, Force Recovery, PWM4, PWM9.

Rev A2

Top Side



Bottom Side

