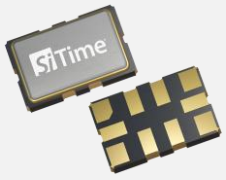
ENDR-TTT

±50 ppb 1 MHz to 105 MHz

Ruggedized Precision Low Power Super-TCXO



5.0 mm x 3.2 mm

Ceramic package

Applications

- Precision GNSS systems
- Mobile low-power systems
- Precision Guided Munitions
- Ballistics, missiles, UAVs
- Military portable radios
- Frequency and phase synchronization systems
- Military, defense, space, avionics systems

Overview

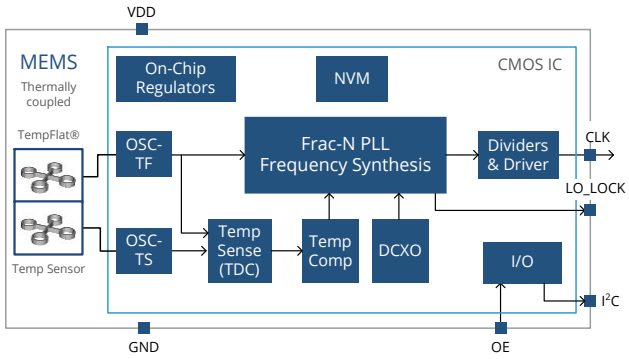
ENDR-TTT is a low-power, low-phase noise, ruggedized ±50 ppb to ±500 ppb precision MEMS Super-TCXO in a 5 mm x 3.2 mm (16 mm^2). Engineered for dynamic performance and low power, the ENDR-TTT is ideal for high reliability defense, avionics, guidance, precision GNSS and communications applications.

Leveraging SiTime's unique DualMEMS® temperature sensing and TurboCompensation® technologies, ENDR-TTT delivers the best dynamic performance for timing stability in the presence of environmental stressors such as airflow, temperature perturbation, vibration, shock, and electromagnetic interference. This device also integrates multiple on-chip regulators to filter power supply noise, eliminating the need for a dedicated external LDO.

The Endura ruggedized clock family provides a lifetime warranty and availability. Refer to Manufacturing Guideline for proper reflow profile and PCB cleaning recommendations to ensure best performance.

Features

- Factory programmed frequency: 1 MHz to 105 MHz
- Low power 20 mW (1.8 V)
- Low phase noise -153 dBc/Hz (Fc=10 MHz, 10 kHz Offset)
- Best dynamic stability under airflow, thermal shock
  - 96,000 *g* Survivability shock
  - 0.004 ppb/*g* acceleration sensitivity
  - ±50 ppb frequency stability over temperature
- -55°C to +125°C operating temperature
- No activity dips or micro jumps
- Digital frequency pulling (DCTCXO) via I^2C or SPI
  - Digital control of output frequency
  - ±200 ppm pull range
  - Frequency pull resolution down to 3.64 ppt
  - Temperature readout
- 1.8 V to 3.3 V supply voltage options
- Unregulated, regulated LVCMOS or clipped sine output
- Lifetime Availability & Warranty
- High-Reliability Production Testing
- COSPAS-SARSAT Gen 1-2 Compliant



ENDR-TTT Block Diagram

Aerospace & Defense

Order samples

TempFlat® MEMS

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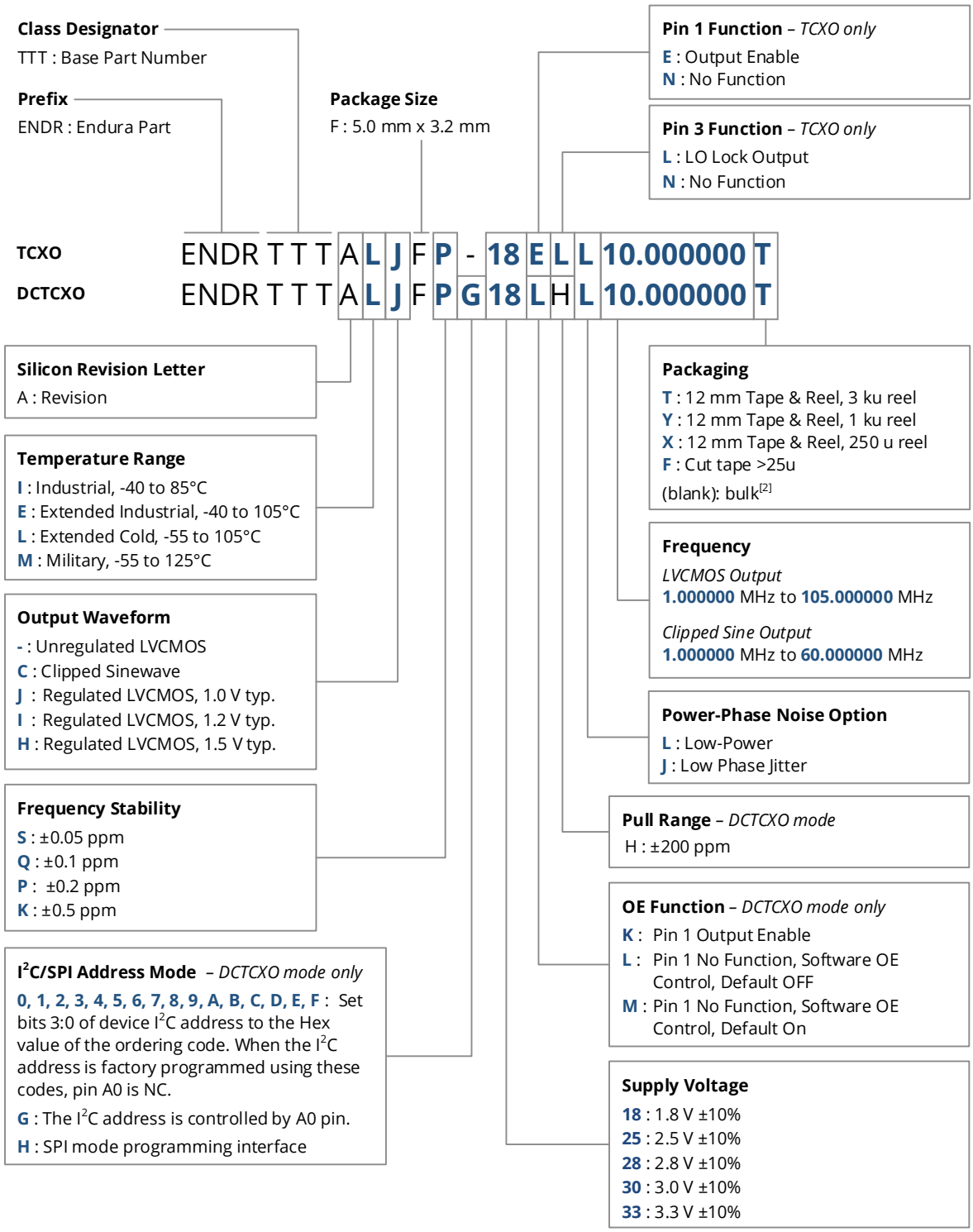
Ordering Information

Part number characters in **blue** represent the customer specific options. The other characters in the part number are fixed.



Notes:

1. "-" corresponds to the default rise/fall time for LVCMOS output as specified in Table 1 (Electrical Characteristics). Contact SiTime for other rise/fall time options for best EMI or driving multiple loads.
2. Bulk is available for sampling only <25 units.

Electrical Specifications

All Min and Max limits are specified over temperature and rated operating voltage unless otherwise stated. Typical values are at 25°C and 1.8 V Vdd.

Table 1. Output Characteristics

Parameters	Symbol	Min.	Typ.	Max.	Unit	Condition
Frequency Coverage						
Nominal Output Frequency Range	F_nom	1	–	105	MHz	LVCMOS Output
		1	–	60		Clipped Sine Output
Temperature Range						
Operating Temperature Range (ambient)	T_use	-55	–	+125	°C	Military, ordering option "M". Contact SiTime for availability
		-55	–	+105	°C	Extended Cold, ordering option "L"
		-40	–	+105	°C	Extended Industrial, ordering option "E"
		-40	–	+85	°C	Industrial, ordering option "I"
Rugged Characteristics						
Acceleration (*g*) sensitivity, Gamma Vector	F_g	–	0.004	0.009	ppb/*g*	Low sensitivity grade; total gamma over 3 axes; 15 Hz to 2 kHz; MIL-PRF-55310, computed per section 4.8.18.3.1
Frequency Stability						
Frequency Stability over Temperature	F_stab	-0.050		0.050	ppm	Referenced to (max frequency + min frequency)/2 over the rated temperature range, stability ordering code "S"
		-0.10	–	0.10		Referenced to (max frequency + min frequency)/2 over the rated temperature range, stability ordering code "Q"
		-0.20		0.20		Referenced to (max frequency + min frequency)/2 over the rated temperature range, stability ordering code "P"
		-0.50	–	0.50		Referenced to (max frequency + min frequency)/2 over the rated temperature range, stability ordering code "K"
Initial Tolerance	F_init	-65	±15	65	ppb	Initial frequency at 25°C at 48 hours after 2 reflows
Supply Voltage Sensitivity	F_Vdd	-	±3	4.5	ppb/V	"L" Low-Power Option, VDD ±100 mV
			±3	8.5		"J" Low-Jitter Option, VDD ±100 mV
Output Load Sensitivity	F_load	-0.9	±0.2	0.9	ppb/pF	**Regulated** Output, Load variation ±10%
		-2.5	±0.3	2.5		**Unregulated** Output, Load variation ±10%
Frequency vs. Temperature Slope	ΔF/ΔT	-2.5		2.5	ppb/°C	"S" 0.05 ppm F_stab option, 0.5°C/min temperature ramp rate
		-3		3		"Q" 0.10 ppm F_stab option, 0.5°C/min temperature ramp rate
		-6		6		"P" 0.20 ppm and "K" 0.5 ppm F_stab option, 0.5°C/min temperature ramp rate
Dynamic Frequency Change during Temperature Ramp	F_dynamic	–	±0.025	–	ppb/s	0.5°C/min temperature ramp rate
Hysteresis Over Temperature	F_hys	-10	±5	10	ppb	0.5°C/min ramp rate, defined as ±ΔF/2.
One-Day Aging	F_1d	-0.5		0.5	ppb	At 85°C, after 30-days of continued operation. Aging is measured with respect to day 31.
One-Year Aging	F_1y	-30		30	ppb	At 85°C, after 2-days of continued operation. Aging is measured with respect to day 3.
10-Year Aging	F_10y	–	±0.4	–	ppm	
20-Year Aging	F_20y	–	±0.5	–	ppm	
Total Frequency Stability Over 20 Years	F_stab_total	–	1.05	–	ppm	0.050 ppm stability option. T_A= 85 C, after 2 days of continued operation. Measured at day 3.
		–	1.12	–	ppm	0.10 ppm stability option. T_A= 85 C, after 2 days of continued operation. Measured at day 3.
		–	1.35	–	ppm	0.20 ppm stability option. T_A= 85 C, after 2 days of continued operation. Measured at day 3.
		-	2	-	ppm	0.5 ppm stability option. T_A= 85 C, after 2 days of continued operation. Measured at day 3.
Allan deviation	ADEV	–	5e-12	–	–	1 and 10 second averaging time, measured 2 hours after startup in a temp chamber with a constant temp, still air

Table 1. Output Characteristics – continued

Parameters	Symbol	Min.	Typ.	Max.	Unit	Condition
Start-up Characteristics						
Start-up Time	T_start	–	–	10	ms	Time to first pulse, measured from the time Vdd reaches 90% of its final value
Output Enable Time	T_oe	–	–	1	µs	F_nom = ≥10 MHz. OE Time will increase for F_o <10 MHz
Time to Rated Frequency Stability	T_stability	–	–	50	ms	Time to first accurate pulse within rated stability, measured from the time Vdd reaches 90% of its final value
Regulated LVCMOS Output Characteristics						
Duty Cycle	DC	45	–	55	%	
Rise/Fall Time	Tr, Tf	–	–	2.0	ns	20% - 80% Vdd, 15 pF Load.
Output Voltage High	VOH	0.90	1.0	1.1	V	Regulated 1.0V
		–	1.2	1.3		Regulated 1.2V
		–	1.5	1.6		Regulated 1.5V
Output Voltage Low	VOL	–	–	0.1	V	
Unregulated LVCMOS Output Characteristics						
Duty Cycle	DC	45	–	55	%	
Rise/Fall Time	Tr, Tf	–	-	2.0	ns	20% - 80% Vdd, 15 pF Load
Output Voltage High	VOH	90%	–	–	Vdd	
Output Voltage Low	VOL	–	–	10%	Vdd	
Output Impedance	Z_out_c	–	39	–	Ω	Impedance looking into output buffer, Vdd = 1.8 V
		–	32	–		Impedance looking into output buffer, Vdd = 3.0 V
		–	31	–		Impedance looking into output buffer, Vdd = 3.3 V
Clipped Sinewave Output Characteristics						
Duty Cycle	DC	45	–	55	%	
Output Voltage Swing	V_out	0.8	–	1.0	V	Clipped sinewave output, 10 kΩ || 10 pF ±10%
Rise/Fall Time	Tr, Tf	1	-	10	ns	20% - 80% Vdd, F_nom = 10 MHz
Local Oscillator Lock (LO_LOCK) LVCMOS Output						
Output Rise-Fall Time, CMOS	Tr_RFL, Tf_RFL	–	2	3.5	ns	10 pF Load
VOH - Output Voltage High	VOH_RFL	75%	–	–	Vdd	10pF Load
VOL - Output Voltage Low	VOL_RFL	–	–	25%	Vdd	10pF Load

Table 2. DC Characteristics

Parameters	Symbol	Min.	Typ.	Max.	Unit	Condition
Supply Voltage						
Supply Voltage	Vdd	1.70	1.8	1.90	V	Option "18"
		2.25	2.5	2.75		Option "25"
		2.52	2.8	3.08		Option "28"
		2.70	3.0	3.30		Option "30"
		2.97	3.3	3.63		Option "33"
Current Consumption Low Power Option						
Current Consumption	Idd	–	11	12	mA	F_nom = 10 MHz, No Load, Vdd = 1.8 V, Max @ 105°C
				13		F_nom = 10 MHz, No Load, Vdd = 1.8 V, Max @ 125°C
OE Disable Current	I_od	–	11	12	mA	OE = GND, output weakly pulled down, Vdd = 1.8 V
Current Consumption Low Jitter Option						
Current Consumption	Idd	–	14	16.5	mA	F_nom = 10 MHz, No Load, Vdd = 1.8 V, Max @ 105°C
				18		F_nom = 10 MHz, No Load, Vdd = 1.8 V, Max @ 125°C
OE Disable Current	I_od		14	16.5	mA	OE = GND, output weakly pulled down, Vdd = 1.8 V

Table 3. Input Characteristics

Parameters	Symbol	Min.	Typ.	Max.	Unit	Condition
Input Characteristics – OE Pin						
Input Impedance	Z_in	75	–	–	kΩ	Internal pull up to Vdd
Input High Voltage	VIH	70%	–	–	Vdd	
Input Low Voltage	VIL	–	–	30%	Vdd	
Frequency Tuning Range – I²C mode						
Pull Range	PR	±200	–	–	ppm	DCTCXO mode
Absolute Pull Range[3]	APR	±5.15	–	–	ppm	±0.1 ppm F_stab, DCTCXO for PR = ±6.25 ppm
		±5.05	–	–	ppm	±0.2 ppm F_stab, DCTCXO for PR = ±6.25 ppm
I²C Interface Characteristics, 200 Ω, 550 pF (Max I²C Bus Load)						
Bus Speed	F_I2C	≤ 400			kHz	-40 to 105°C, -55°C to +125°C
		≤ 1000			kHz	-40 to 85°C (Contact SiTime)
Input Voltage Low	VIL_I2C	–	–	30%	Vdd	DCTCXO mode
Input Voltage High	VIH_I2C	70%	–	–	Vdd	DCTCXO mode
Output Voltage Low	VOL_I2C	–	–	0.1	V	DCTCXO mode
Input Leakage current	I_L	10	–	30	µA	0.1 V_{DD}< VOUT < 0.9 V_{DD}. Includes typical leakage current from 200 kΩ pull resistor to VDD. DCTCXO mode
Input Capacitance	C_{IN}	–	–	11	pF	DCTCXO mode

Note:

3. APR = PR – F_init - F_20y - F_stab (Absolute Pull Range is the Pull Range minus initial tolerance minus 20-year aging minus frequency stability over temperature)

Table 4. Low-Power Option "L" Jitter & Phase Noise Over Temperature at 10 MHz

Parameters	Symbol	Min.	Typ.	Max.	Unit	Condition
Jitter						
RMS Phase Jitter	T_jitt_ph	–	1.15	1.5	ps	F_nom = 10 MHz, 12 kHz – 5 MHz offset
Phase Noise						
1 Hz offset		–	-87	-86	dBc/Hz	F_nom = 10 MHz, measured over temperature
10 Hz offset		–	-114	-113	dBc/Hz	
100 Hz offset		–	-134	-132	dBc/Hz	
1 kHz offset		–	-146	-145	dBc/Hz	
10 kHz offset		–	-151	-150	dBc/Hz	
100 kHz offset		–	-150	-149	dBc/Hz	
1 MHz offset		–	-150	-148	dBc/Hz	
Spurious Phase Noise	T_spur	–	-	-87	dBc	F_nom = 10 MHz, 50 Hz to 5 MHz offsets
Power Supply Noise Spur						
Power Supply Ripple	T_PSspur	–	–	-90	dBc	10 mV peak-to-peak sinusoidal power supply noise (50 Hz to 5 MHz). Applies to regulated output VOH ≤ 1.0

Table 5. Low-Power Option "L" Jitter & Phase Noise Over Temperature at 100 MHz

Parameters	Symbol	Min.	Typ.	Max.	Unit	Condition
Jitter						
RMS Phase Jitter	T_jitt_ph	–	1.15		ps	F_nom = 100 MHz, 12 kHz – 20 MHz offset
Phase Noise						
1 Hz offset		–	-67	–	dBc/Hz	F_nom = 100 MHz
10 Hz offset		–	-94	–	dBc/Hz	
100 Hz offset		–	-114	–	dBc/Hz	
1 kHz offset		–	-125	–	dBc/Hz	
10 kHz offset		–	-131	–	dBc/Hz	
100 kHz offset		–	-131	–	dBc/Hz	
1 MHz offset		–	-131	–	dBc/Hz	
Spurious Phase Noise	T_spur	–	-	-70	dBc	F_nom = 100 MHz, 50 Hz to 20 MHz offsets
Power Supply Noise Spur						
Power Supply Ripple	T_PSspur	–	–	-70	dBc	10 mV peak-to-peak sinusoidal power supply noise (50 Hz to 20 MHz). Applies to regulated output VOH ≤ 1.0

Table 6. Low-Phase Jitter Option "J" Jitter & Phase Noise Over Temperature at 10 MHz

Parameters	Symbol	Min.	Typ.	Max.	Unit	Condition
Jitter						
RMS Phase Jitter	T_jitt_ph	–	0.80		ps	F_nom = 10 MHz, 12 kHz – 5 MHz offset
Phase Noise						
1 Hz offset		–	-85	–	dBc/Hz	F_nom = 10 MHz
10 Hz offset		–	-113	–	dBc/Hz	
100 Hz offset		–	-131	–	dBc/Hz	
1 kHz offset		–	-148	–	dBc/Hz	
10 kHz offset		–	-153	–	dBc/Hz	
100 kHz offset		–	-154	–	dBc/Hz	
>1 MHz offset		–	-156	–	dBc/Hz	
Spurious Phase Noise	T_spur	–	-	-90	dBc	F_nom = 10 MHz, 50 Hz to 5 MHz offsets
Power Supply Noise Spur						
Power Supply Ripple	T_PSspur	–	–	-90	dBc	10 mV peak-to-peak sinusoidal power supply noise (50 Hz to 5 MHz). Applies to regulated output VOH ≤ 1.0

Table 7. Low-Phase Jitter Option "J" Jitter & Phase Noise Over Temperature at 100 MHz

Parameters	Symbol	Min.	Typ.	Max.	Unit	Condition
Jitter						
RMS Phase Jitter	T_jitt_ph	–	0.80	1.2	ps	F_nom = 100 MHz, 12 kHz – 20 MHz offset
Clipped Sine Phase Noise						
1 Hz offset		–	-69	-64	dBc/Hz	F_nom = 100 MHz
10 Hz offset		–	-97	-94	dBc/Hz	
100 Hz offset		–	-115	-114	dBc/Hz	
1 kHz offset		–	-131	-128	dBc/Hz	
10 kHz offset		–	-134	-132	dBc/Hz	
100 kHz offset		–	-132	-130	dBc/Hz	
1 MHz offset		–	-136	-132	dBc/Hz	
Spurious Phase Noise	T_spur	–	-	-69	dBc	F_nom = 100 MHz, 50 Hz to 20 MHz offsets
Power Supply Noise Spur						
Power Supply Ripple	T_PSspur	–	–	-70	dBc	10 mV peak-to-peak sinusoidal power supply noise (50 Hz to 20 MHz). Applies to regulated output VOH ≤ 1.0

Table 8. Absolute Maximum Limits

Attempted operation outside the absolute maximum ratings may cause permanent damage to the part.
Actual performance of the IC is only guaranteed within the operational specifications, not at absolute maximum ratings.

Parameter	Test Conditions	Value	Unit
Storage Temperature		-65 to 150	°C
Power Supply Voltage Range (Vdd)		-0.5 to 4	V
Human Body Model (HBM) ESD Protection	JESD22-A114	2000	V
Soldering Temperature (follow standard Pb-free soldering guidelines)		260	°C
Junction Temperature[4]		130	°C

Note:
4. Exceeding this temperature for an extended period of time may damage the device.

Table 9. Thermal Considerations[5,6]

Package	ΘJA (°C/W) [5]	ΘJB, Board (°C/W)	ΘJC, Top (°C/W)	ΨJT (°C/W)
Ceramic 5.0 mm x 3.2 mm	59	10	29	13

Note:
5. Simulated in still air. Refer to JESD51 for θJA, θJB, θJC, and ΨJT definitions.
6. Devices soldered on a JESD51 2s2p compliant board.

Table 10. Maximum Operating Junction Temperature

Maximum Operating Temperature (ambient)	Maximum Operating Junction Temperature
105°C	125°C
125°C	130°C

Table 11. Environmental Compliance

Parameter	Test Conditions	Value	Unit
Mechanical Shock Resistance	**MIL-STD-883F, Method 2002, condition G**	30,000	*g*
Mechanical Survivability	**High-g air gun, X-, Y-, and Z-axis orientations**	96,000	*g*
Mechanical Vibration Resistance	**MIL-STD-883F, Method 2007**	70	*g*
Acceleration (g) sensitivity, Gamma Vector	**Low sensitivity grade; total gamma over 3 axes; 15 Hz to 2 kHz; MIL-PRF-55310, computed per section 4.8.18.3.1**	0.009	ppb/*g*
Temperature Cycle	**JESD22, Method A104**	–	–
Solderability	**MIL-STD-883F, Method 2003**	–	–
Moisture Sensitivity Level	**MSL1 @260°C**	–	–

Typical Performance Plots

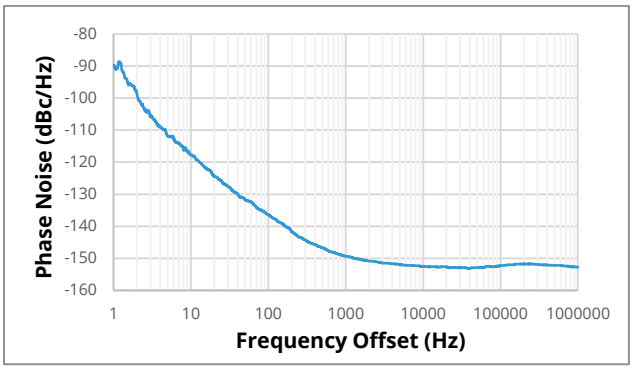


Figure 1. ENDR-TTT Phase Noise – 10 MHz Fc

Device Pin-outs

Pin-out Top Views

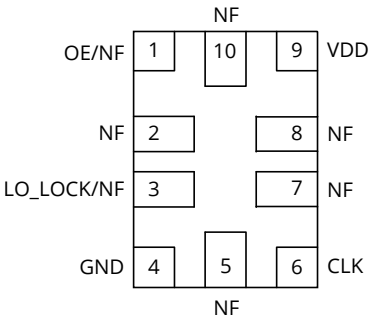


Figure 2. TCXO

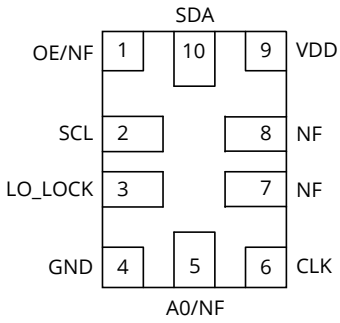


Figure 3. DCTCXO (I2C)

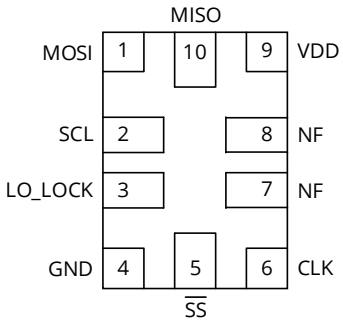


Figure 4. DCTCXO (SPI)

Table 12. Pin Description

Pin	Symbol	I/O	Internal Pull-up/ Pull Down Resistor	Function
1	OE	OE – Input	>70 kΩ Pull-Up	H: specified frequency output L: output is high impedance. Only output driver is disabled
	NF	NF[7] – No Function	–	H or L or Open: No effect on output frequency or other device functions
	MOSI	SPI Input	100 kΩ Pull-Up	SPI Serial data input, DCTCXO only
2	SCL	SCL – Input	200 kΩ Pull-Up	SPI and I²C serial clock input, DCTCXO only
	NF[7]	No Function	-	H or L or Open: No effect on output frequency or other device functions
3	LO_LOCK/NF[7]	LO_LOCK - Output	–	Local Oscillator (LO) Lock Indicator. 0 = oscillator not locked 1 = oscillator locked
		NF[7] – No Function	–	H or L or Open: No effect on output frequency or other device functions
4	GND	Power	–	Connect to ground
5	A0	I2C Input	100 kΩ Pull-Up	Device I²C address when the address selection mode is via the A0 pin. This pin is NC when the I²C device address is specified in the ordering code. See Tables 19 and 20.
	$\overline{SS}$	SPI Input	100 kΩ Pull-Up	SPI chip-select, active LOW
	NF	NF[7] – No Function	–	H or L or Open: No effect on output frequency or other device functions.
6	CLK	Output	–	LVCMOS, or clipped sinewave oscillator output
7	NF[8]	No Function	–	H or L or Open: No effect on output frequency or other device functions
8	NF[8]	No Function	–	H or L or Open: No effect on output frequency or other device functions
9	VDD	Power	–	Connect to power supply A 0.1 µF capacitor in parallel with a 10 µF capacitor are required between VDD and GND. The 0.1 µF capacitor is recommended to place close to the device and place the 10 µF capacitor less than 2 inches away.
10	SDA	I2C – Input	200 kΩ Pull Up	I²C Serial data input
	MISO	SPI Output	200 kΩ Pull-Up	SPI serial data output

Notes:

7. In OE mode for noisy environments, a pull-up resistor of 10 kΩ or less is recommended if pin 1 is not externally driven. If pin 1 needs to be left floating, use the NC option.
8. All NF pins can be left floating. It is recommended to solder them down.

Schematic Example

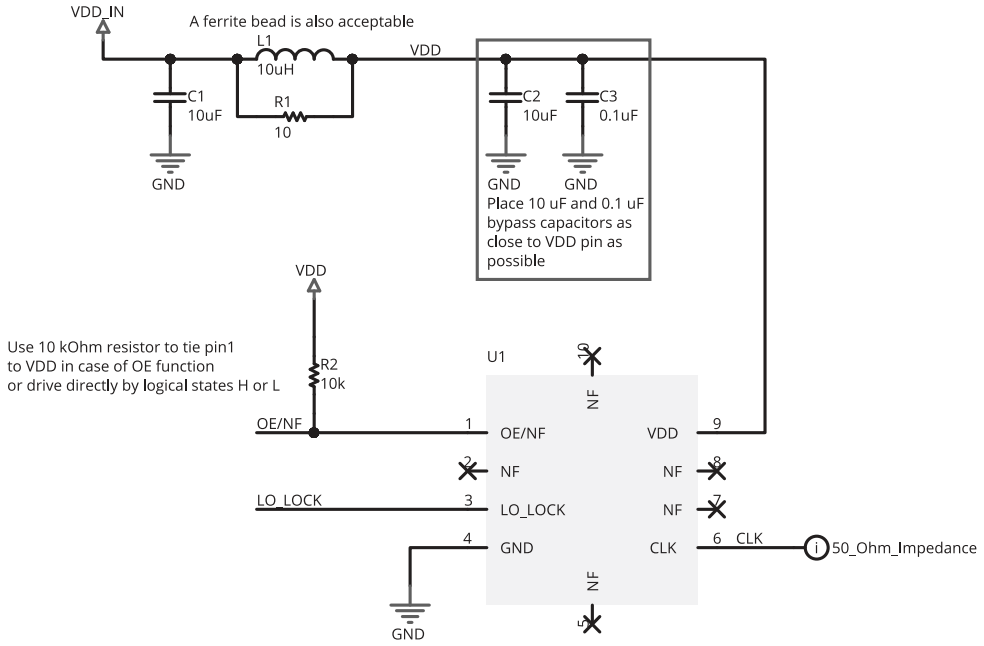


Figure 5. Schematic Example TCXO

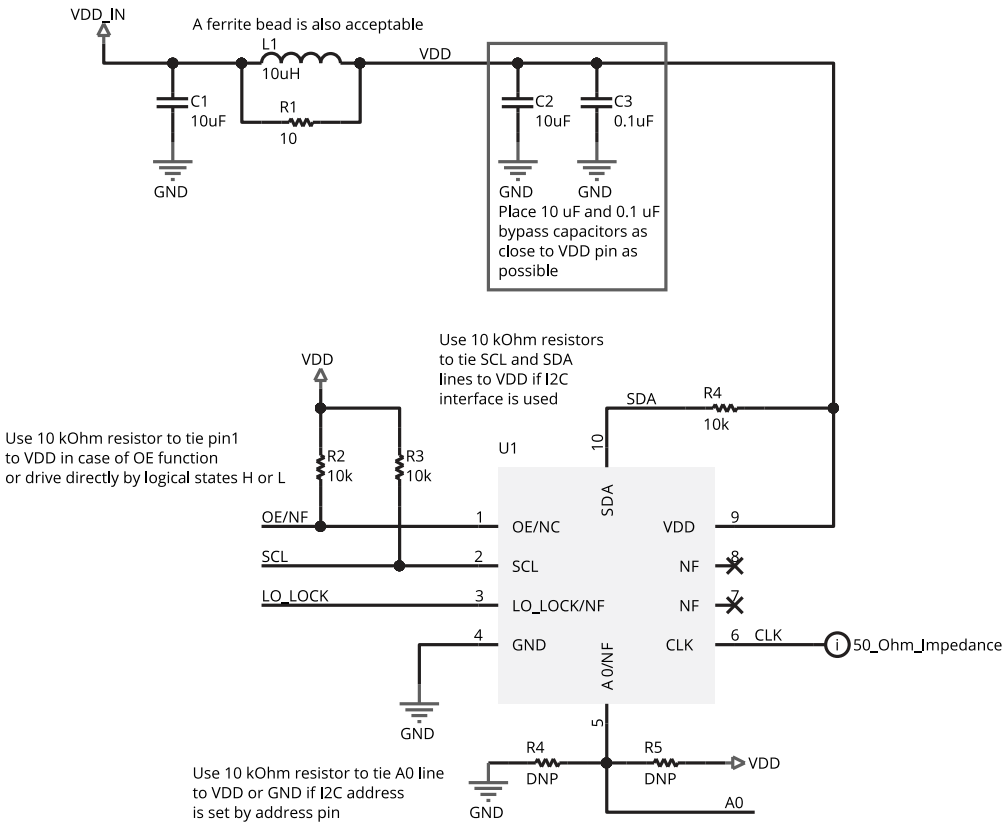


Figure 6. Schematic Example DCTCXO (with LO_Lock)

Layout Example

TCXO

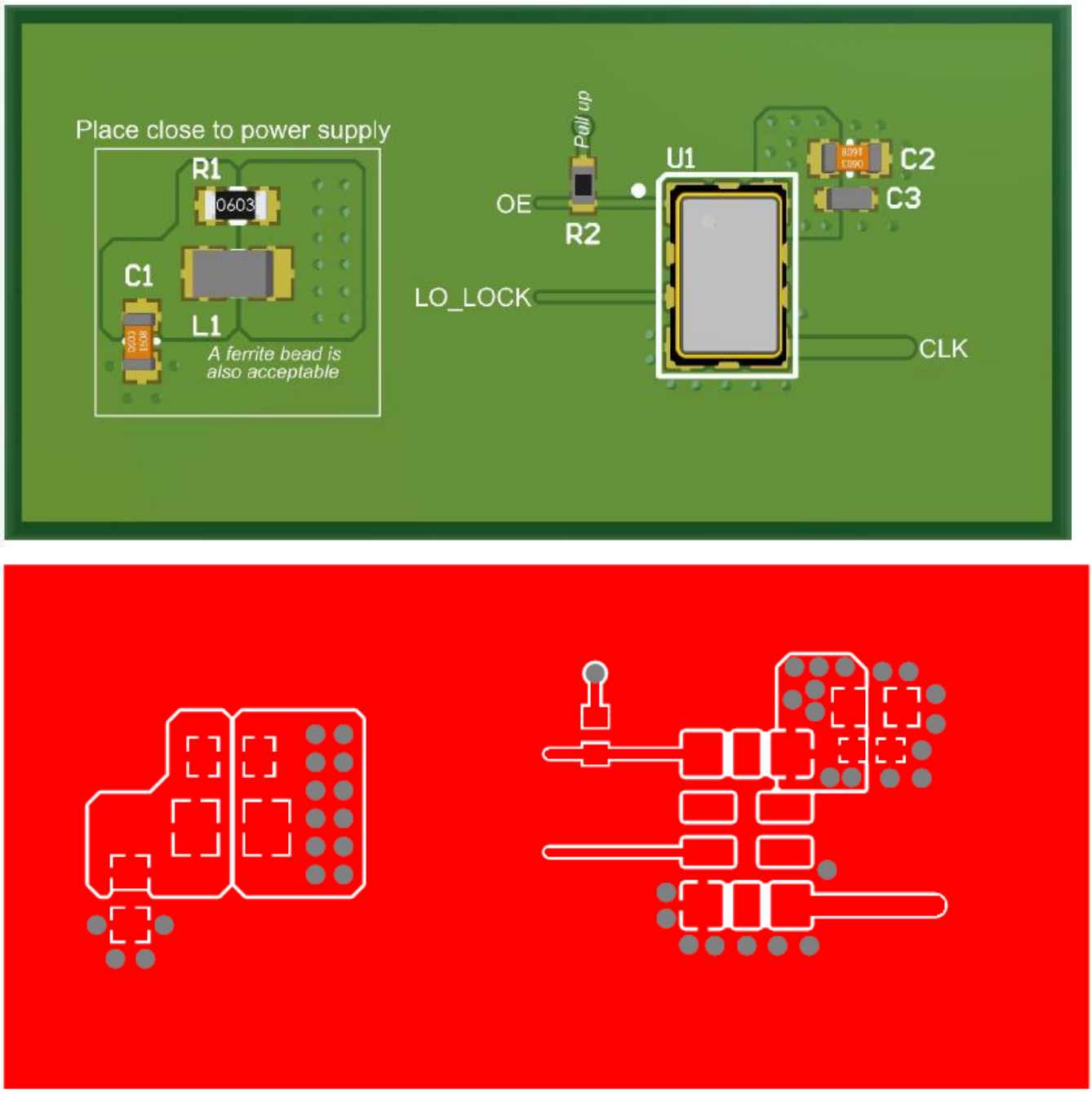


Figure 7. Layout Example (TCXO)

DCTCXO

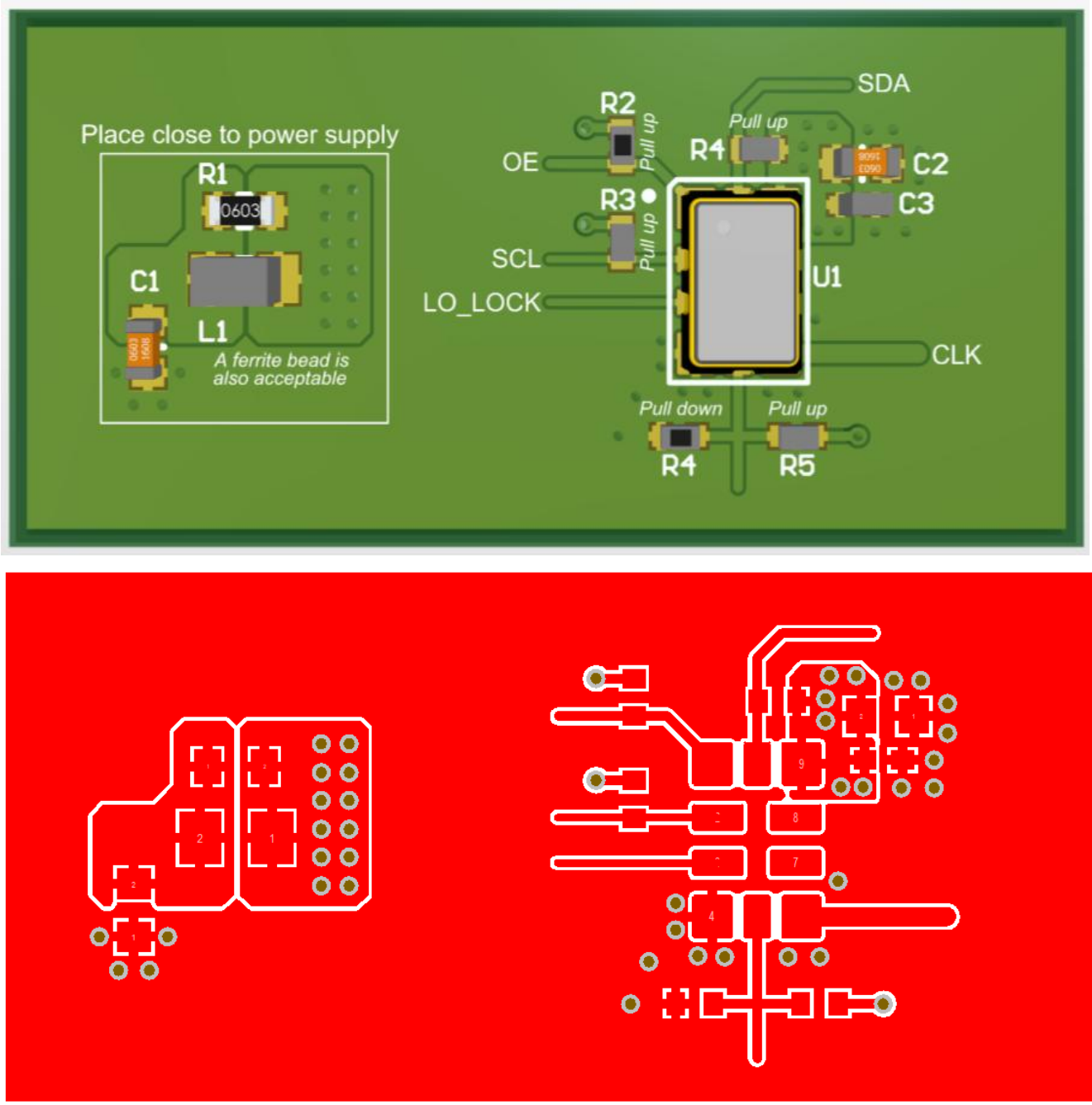


Figure 8. Layout Example (DCTCXO)

Waveforms

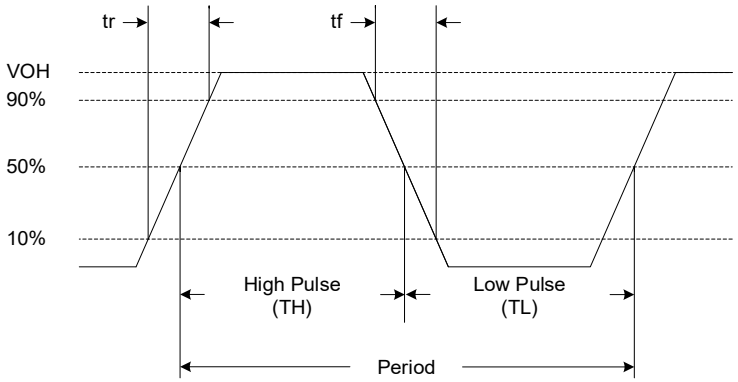


Figure 9. Regulated LVCMOS Waveform Diagram

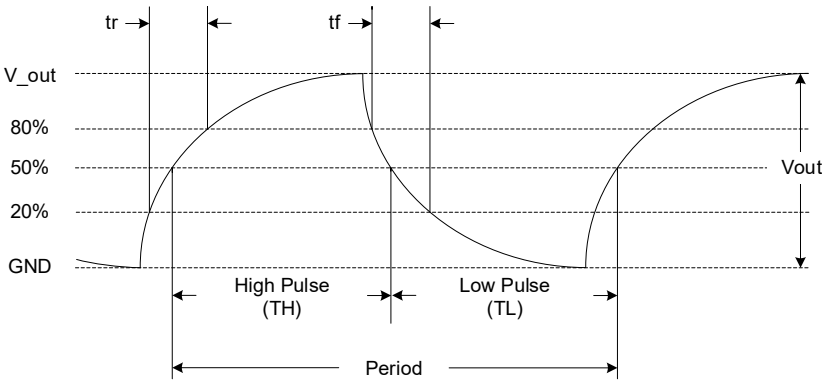


Figure 10. Clipped Sinewave Waveform Diagram

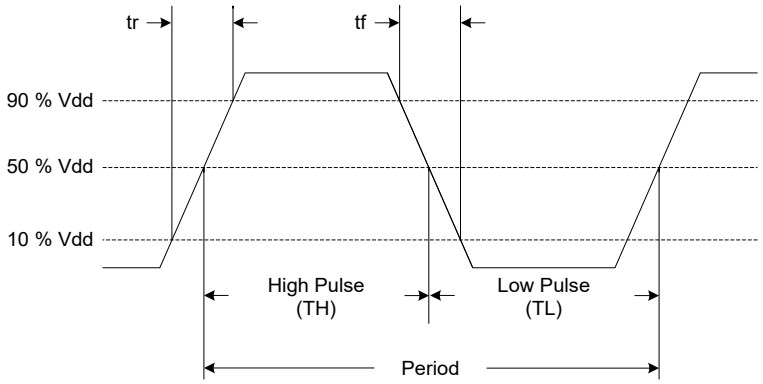


Figure 11. LVCMOS Waveform Diagram

Note:

9. Duty Cycle is computed as Duty Cycle = TH/Period.

Architecture Overview

Based on SiTime's innovative Super-TCXO Platform, ENDR-TTT delivers exceptional dynamic performance, i.e. resilience to environmental stressors such as shock, vibration, and fast temperature transients. Underpinning SiTime Super-TCXO Platform are SiTime's unique DualMEMS® temperature sensing architecture and TurboCompensation® technologies.

DualMEMS is a noiseless temperature compensation scheme. It consists of two MEMS resonators fabricated on the same die substrate. The TempFlat® MEMS resonator is designed with a flat frequency characteristic over temperature whereas the temperature sensing resonator is by design sensitive to temperature changes. The ratio of frequencies between these two resonators provides an accurate reading of the resonator temperature with 20 µK resolution.

By placing the two MEMS resonators (TempFlat MEMS® and temperature sensing resonator) on the same die, this temperature sensing scheme eliminates any thermal lag and gradients between resonator and temperature sensor, thereby overcoming an inherent weakness of legacy quartz TCXOs.

The DualMEMS temperature sensor drives a state-of-the-art CMOS temperature compensation circuit. The TurboCompensation design, with >100 Hz compensation bandwidth, achieves a dynamic frequency stability that is far superior to any quartz TCXO. The digital temperature compensation enables additional optimization of frequency stability and frequency slope over temperature within any chosen temperature range for a given system design.

For more information regarding the product and its benefits please visit:

- SiTime's breakthroughs section
- TechPaper: DualMEMS Temperature Sensing Technology
- TechPaper: DualMEMS Resonator TDC

Functional Overview

ENDR-TTT is designed for maximum flexibility with an array of factory programmable options, enabling system designers to configure this precision device for optimal performance in a given application.

Frequency Stability

ENDR-TTT comes in four factory-trimmed stability grades that are optimized for different applications.

Table 13. Stability Grades vs. Ordering Codes

Frequency Stability Over Temperature	Ordering Code
±0.050 ppm	S
±0.1 ppm	Q
±0.2 ppm	P
±0.500 ppm	K

Output Frequency and Format

ENDR-TTT can be factory programmed for an output frequency without sacrificing lead time or incurring an upfront customization cost typically associated with custom-frequency quartz TCXOs.

The device supports both LVCMOS and clipped sinewave output. Ordering codes for the output format are shown below:

Table 14. Output Formats vs. Ordering Codes

Output Format	Ordering Code
Regulated LVCMOS	J for 1.0 V VOH typical I for 1.2 V VOH typical H for 1.5 V VOH typical
Unregulated LVCMOS	"-"
Clipped Sinewave	"C"

Contact SiTime for other VOH for Regulated LVCMOS.

Output Frequency Tuning

In addition to the non-pullable TCXO, ENDR-TTT can also support output frequency tuning through I^2C or SPI interface (DCTCXO). The I^2C interface enables factory programmed pull-range option of ±200 ppm.

Refer to Device Configuration section for details.

Pin 1 Configuration (OE or NC)

Pin 1 of ENDR-TTT can be factory programmed to support two modes: Output Enable (OE), or No Connect (NC).

Table 15. Pin Configuration Options

Pin 1 Configuration	Operating Mode	Output
OE	TCXO/DCTCXO	Active or High-Z
NC	TCXO/DCTCXO	Active

When pin 1 is configured as OE pin, the device output is guaranteed to operate in one of the following two states:

- Clock output with the frequency specified in the part number when Pin 1 is pulled to logic high
- Hi-Z mode with weak pull down when pin 1 is pulled to logic low.

When pin 1 is configured as NC, the device is guaranteed to output the frequency specified in the part number at all times, regardless of the logic level on pin 1.

Device Configurations

ENDR-TTT supports 2 device configurations – TCXO, and DCTCXO. The TCXO is directly compatible with quartz TCXOs. The DCTCXO configuration provides performance enhancement by eliminating VCTCXO's sensitivity to control voltage noise with an I^2C/SPI digital interfaces for frequency tuning.

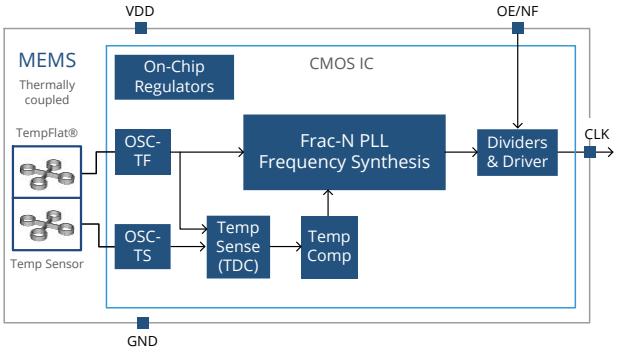


Figure 12. Block Diagram – TCXO

TCXO Configuration

The TCXO generates a fixed frequency output, as shown in Figure 12. The frequency is specified by the user in the frequency field of the device ordering code and then factory programmed. Other factory programmable options include supply voltage, output types (Regulated and unregulated LVCMOS or clipped sinewave), and pin 1 functionality (OE or NC).

Refer to the Ordering Information section at the end of the datasheet for a list of all ordering options.

LO_Lock Functional Description

When selected in part ordering information, LO_Lock is an output indicating the health of the output clock signal after self-check of NVM, MEMS oscillator and PLL status. After power-on reset, when a failure is detected, the impaired clock will continue running. LO_Lock output is a push/pull driver with High when the clock is locked (ie running properly) and Low when the clock is not running properly. When the fault clears, the LO_Lock output will be reset to a logic High. The LO_Lock function is always ON for the DCTCXO. The TCXO option can select between LO_Lock function and no-function on pin 3.

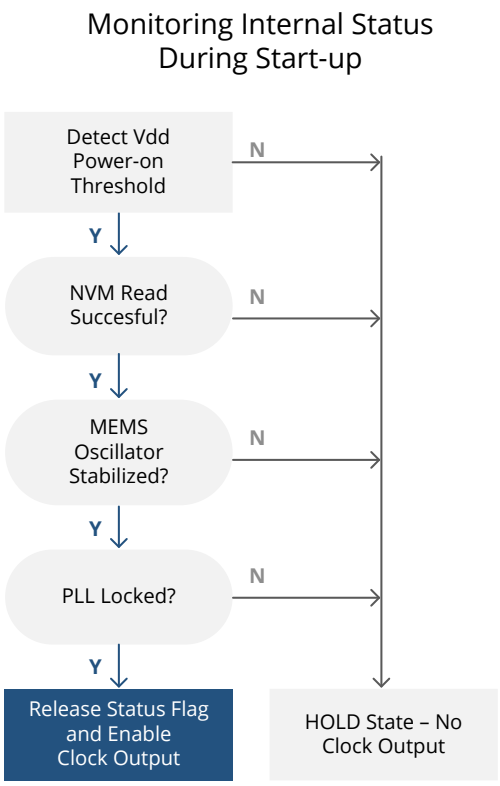


Figure 13. LO_Lock Functional Diagram

DCTCXO Configuration

ENDR-TTT offers digital control of the output frequency, as shown in Figure 14. The output frequency is controlled by writing frequency control words over the I²C interface.

There are several advantages of DCTCXOs relative to VCTCXOs:

1. Frequency control resolution as low as 3.64E-15. This high resolution minimizes accumulated time error in synchronization applications.
2. Lower system cost – A VCTCXO may need a Digital to Analog Converter (DAC) to drive the control voltage input. In a DCTCXO, the frequency control is achieved digitally by register writes to the control registers via I²C/SPI, thereby eliminating the need for a DAC.
3. Better noise immunity – The analog signal used to drive the voltage control pin of a VCTCXO can be sensitive to noise, and the trace over which the signal is routed can be susceptible to noise coupling from the system. The DCTCXO does not suffer from analog noise coupling since the frequency control is performed digitally through I²C/SPI.
4. No frequency-pull non-linearity – The frequency pulling is achieved via fractional feedback divider of the PLL, eliminating any pull non-linearity concerns typical of quartz-based VCTCXOs. This improves dynamic performance in closed-loop applications.
5. Programmable wide pull range – The DCTCXO pulling mechanism is via the fractional feedback divider and is therefore not constrained by resonator pullability as in quartz-based solutions.

This section further provides more information on critical DCTCXO parameters including pull range, absolute pull range, frequency output, and control registers.

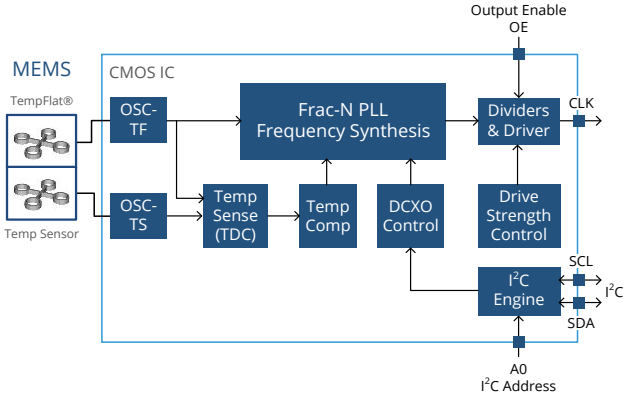


Figure 14. Block Diagram (on example of I²C interface)

Pull Range, Absolute Pull Range

Pull range (PR) is the amount of frequency deviation that will result from changing the control word over its maximum range under nominal conditions.

Absolute pull range (APR) is the guaranteed controllable frequency range over all environmental and aging conditions. Effectively, it is the amount of pull range remaining after taking into account frequency stability and tolerances over variables such as temperature, power supply voltage, and aging, i.e.:

$$\text{APR} = \text{PR} - F_{\text{stability}} - F_{\text{aging}}$$

where $F_{\text{stability}}$ is the device frequency stability due to initial tolerance and variations on temperature, power supply, and load. In the case of the Low Power ENDRTTT TCXO $F_{\text{stability}}$ and F_{aging} are insignificant compared to PR, meaning the APR is essentially equal to PR.

Figure 15 shows a typical SiTime DCXO Freq vs Frequency Control Word (FCW) characteristic. The Frequency vs FCW characteristic varies with conditions, so that the frequency output at a given FCW can vary by as much as the specified frequency stability of the DCXO. For such DCXOs, the frequency stability and APR are independent of each other. This allows very wide range of pull options without compromising frequency stability.

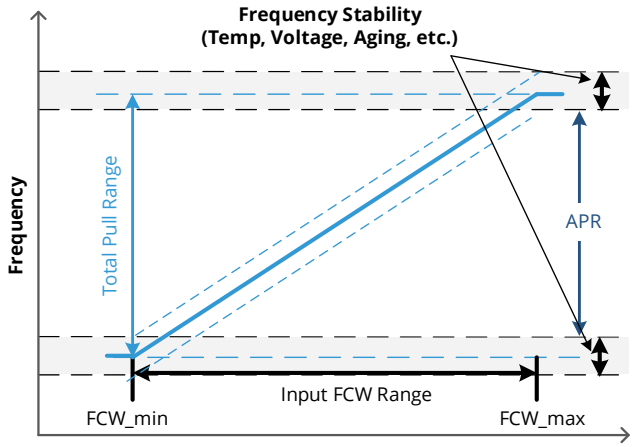


Figure 15. Typical SiTime DCTCXO Frequency vs FCW plot

The FCW_min and FCW_max are the specified limits of the FCW range as shown in Figure 15 above. Applying FCW values beyond the upper and lower limits does not result in significant changes of output frequency. The frequency vs FCW characteristic of the DCXO saturates beyond the FCW_min and FCW_max limits.

Pull range and absolute pull range are described in the previous section. Table 16 below shows the pull range and corresponding APR values for each of the frequency vs. temperature ordering options.

Table 16 below shows the pull range and corresponding APR values for each of the frequency vs. temperature ordering options.

Table 16. APR Options

Pull Range Ordering Code	Pull Range (ppm)	APR ppm ±0.05 ppm option includes 20-year aging	APR ppm ±0.1 ppm option includes 20-year aging	APR ppm ±0.2 ppm option includes 20-year aging	APR ppm ±0.5 ppm option includes 20-year aging
1.2	±200	198.95 ppm	198.9 ppm	198.8 ppm	198 ppm

Notes:
10. APR includes initial tolerance, frequency stability vs. temperature, and the indicated 20-year aging.

Output Frequency

The device powers up at the nominal operating frequency and pull range specified by the ordering code. After power-up, the output frequency can be controlled via the respective control registers. The maximum output frequency change is constrained by the pull range limits.

The pull range for the ±200 ppm ordering code is fixed to ±200 ppm with the actual pulling value being a ratio of this range determined by one fixed point control word.

The control word can be factory-programmed with an accurate decimal clipping limit between 0 and 0.25, corresponding to a ±0 ppm and ±200 ppm pull range (See Table 17 for resolution). A graphical depiction of clipping is shown below in Figure 16.

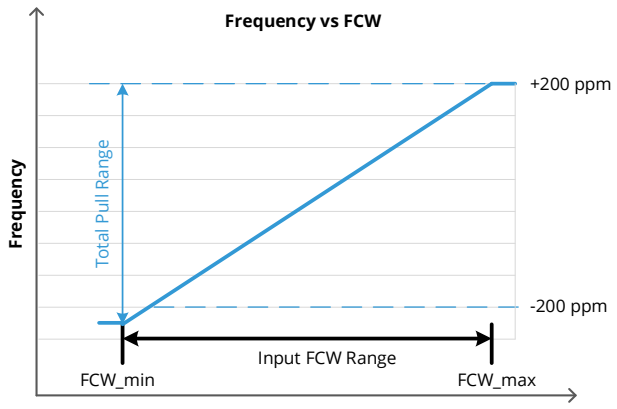


Figure 16. DCTCXO_Clip Illustration

The ppm frequency offset is specified by the 39 bit DCTCXO frequency control word (**FCW**) in two's complement format as described in the I²C/SPI Register Descriptions. The power up default value is 00000000...00000000b (all zeros) which sets the output frequency at its nominal value (0 ppm).

The FCW should be written from LSW to MSW; a frequency change is initiated after the MSW value is written to either pull range value register. To change the output frequency, a frequency control word is first written to 0x04[15:0] (Least Significant Word), then to 0x05[15:0] (Middle Word) and lastly 0x06[6:0] (Most Significant Word).

The frequency output is specified by the value loaded in the DCTCXO register. The output frequency, F_{OUT}, is determined by the equation below, where F_{NOM} is the nominal frequency with no pull. DCTCXO_frac is a signed 39 bit fraction, where the most significant bit represents the sign and the remaining 38 bits represent the fraction, the total range of which is ±0.25. Values exceeding ±0.25 will be clipped as follows:

$$F\_out = \left(1 + \min(0.25, DCXO\_frac) \times 800e^{-6}\right) F\_nom$$

Table 17 below shows the frequency resolution versus pull range programmed.

Table 17. Frequency Resolution versus Pull Range

Programmed Pull Range	Frequency Resolution	Clipping Resolution
±200 ppm	2.91×10^{-15}	9.76×10^{-8}

Figure 17 shows how the two's complement signed value of Frequency Control Word (FCW) 1 sets the output frequency within the clipped ±200 ppm pull range. Therefore, to set the desired output frequency, one just needs to calculate the fraction of full-scale value ppm, convert to two's complement binary, and then write these values to the frequency control word register rows.

Bits	38:36	35:32	31:28	27:24	23:20	19:16	15:12	11:8	7:4	3:0
Hex	010	0000	0000	0000	0000	0000	0000	0000	0000	0000
Decimal	(2^36)-1 = 68,719,476,735									
ppm	+200 ppm									

Bits	38:36	35:32	31:28	27:24	23:20	19:16	15:12	11:8	7:4	3:0
Hex	000	0000	0000	0000	0000	0000	0000	0000	0000	0000
Decimal	0									
ppm	0 ppm									

Bits	38:36	35:32	31:28	27:24	23:20	19:16	15:12	11:8	7:4	3:0
Hex	111	0000	0000	0000	0000	0000	0000	0000	0000	0000
Decimal	(2^36) = -68,719,476,735									
ppm	-200 ppm									

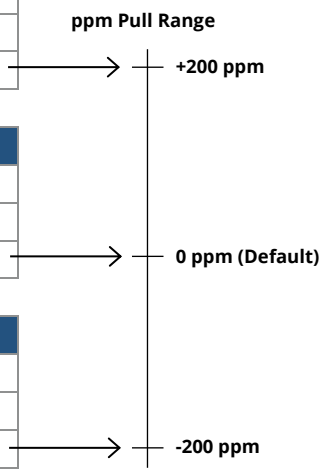


Figure 17: Frequency Control Word

The following formula generates the control word value:

Control word value = ROUND((2^{38}-1) × ppm shift from nominal/pull range), where RND is the rounding function which rounds the number to the nearest whole number.

2 examples follow. Examples 1 and 2 cover the case where DCXO_Clip=0.25 following factory programming. In this case the full pull range is ±200 ppm.

Example 1:

- Default Output Frequency = 19.2 MHz
- Desired Output Frequency = 19.201728 MHz (+90 ppm)

Fractional value required for +90 ppm can be calculated as follows:

- 90 ppm / 800 ppm × (2^{38}-1) = 30,923,764,531.0875.

Rounding to the nearest whole number yields 30,923,764,531 and converting to two's complement gives a binary value of, 0111 0011 0011 0011 0011 0011 0011 0011 or 733333333 in hex.

Example 2:

- Default Output Frequency = 10 MHz
- Desired Output Frequency = 9.9995 MHz (-50 ppm)

Following the formula shown above,

- (-50 ppm / 800 ppm) × (2^{38}) = -17,179,869,184.

Converting this to two's complement binary results in -1*(000 0100 0000 0000 0000 0000 0000 0000 0000) = 111 1100 0000 0000 0000 0000 0000 0000 0000 0000, or 3C00000000 in hex. The negative number is represented as a 2's complement.

Temperature Read

Endura™ Ruggedized Precision Low Power Super TCXO products include a temperature readout option that permits reading a temperature-to-digital-converter's (TDC) data from the device via an I²C/SPI interface. This TDC data specifies the internal ambient temperature that the MEMS resonator operates at. This data can be used by a system to further improve the frequency-over-temperature stability performance of the device.

All the necessary details for reading and interpreting the TDC data are provided below.

Operation Overview

Figure 18 shows the block diagram of an Elite Super-TCXO oscillator with temperature readout functionality.

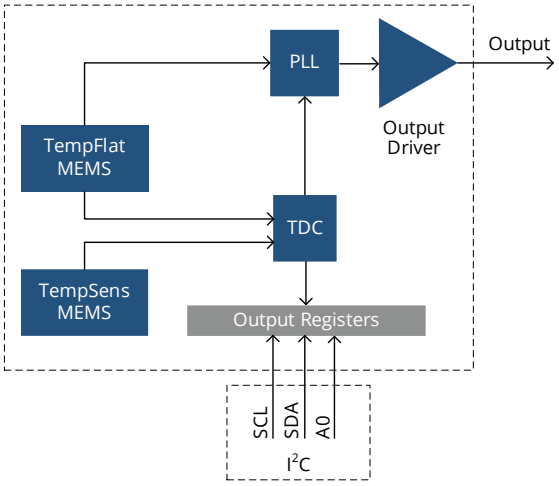


Figure 18: SiTime Super TCXO with temperature readout (based on I²C example)

After the device starts up, the TDC tracks temperature changes that are used as inputs to the device's internal compensation algorithm. In parallel, the same TDC data is made available in the I²C/SPI accessible output registers.

The TDC data goes through a digital low-pass filter, so a user should wait until the filter output settles before reading back and using the TDC data (see Figure 19).

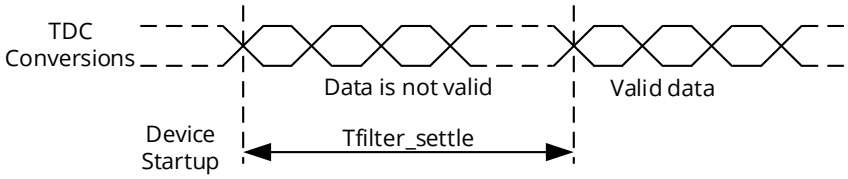


Figure 19. TDC filter output settling

Temperature Readout Operation

The TDC data can be read back at different resolutions:

1. 49-bit full resolution
2. 33/17-bit reduced resolution, available to balance readout resolution with readout time

The TDC data is derived from the relative frequency change of the MEMS resonator due to its change in temperature, and can be converted to absolute degrees Celcius. Conversion from the data format provided to absolute temperature will be covered in subsequent sections.

The TDC data is accessible by the combination of four 16-bit output registers (addresses 0x3B, 0x3C, 0x3D and 0x3E). Higher numbered addresses contain higher valued bits. Lower numbered addresses can be ignored to save readout time at the cost of readout resolution. Register writing by the on-chip temperature calculator is paused for the duration of an I^2C/SPI read, therefore it is recommended to read the desired amount of rows in a single operation. No guarantee can be given that subsequent individual I^2C/SPI reads return data from the same temperature calculation cycle.

The sequence for reading registers is as follows:

1. Address 0x3B/59: LSW of the 49-bit full resolution TDC data. Start a burst read from this address for full resolution capture, providing bits [15:0] of the 49-bit value.
2. Address 0x3C/ 60: Intermediate 16-bit word of the 49-bit full resolution TDC data, providing bits [31:16]. Start here when reading the 33-bit data format.
3. Address 0x3D/ 51: Intermediate 16-bit word of the 49-bit full resolution TDC data, providing bits [47:32]. Start here when reading the 17-bit data format.
4. Address 0x3F/ 62: Contains the MSB of the 49-bit value in the LSB of the word. All other bits will read zero.

49-bit Resolution Mapping

For 49-bit resolution temperature readout, the full 16-bit data from Address 0x3B, 0x3C, 0x3D and the MSB in 0x3E are used.

TDC data is formatted as a s.2i.46f fixed point two's complement value. The 49 bits are stored in little-endian format, therefore bit [48] stores the sign bit, bits [47:46] store the integer bits, and bits [45:0] store the fractional bits. This value corresponds to the estimated absolute temperature of the MEMS resonator and can be converted to (a) and from (b) degrees Celsius as follows:

a. From TDC data to degrees C:

$$T = 65(TDC + 2.5) - 137.5 \quad \text{Eq. 1}$$

b. From degrees C to TDC data:

$$TDCRead = -2.5 + (T + 137.5)/65 \quad \text{Eq. 2}$$

Conversion from raw readout bits to a decimal format of TDC data follows normal fixed point arithmetic rules that involve casting of read bits to a signed integer/floating point notation and scaling to accommodate the fixed-point portion:

TDCRead_scaled = $**signed** (TDCRead) / 2^46 Eq. 3

33-bit Resolution Mapping

For 33-bit TDC readout starting from Address 0x3C, TDC data will be formatted as s.2i.30f, dropping off 16 LSBs. Calculations are equivalent to the 49-bit mapping, except that scaling must be adjusted to match the number of fractional bits readout: 2^30f.

17-bit Resolution Mapping

For 17-bit TDC readout starting from Address 0x3D, TDC data will be formatted as s.2i.14f. Calculations are equivalent to the 49-bit mapping, except that scaling must be adjusted to match the number of fractional bits readout: 2^14f.

Register Map and Serial Interface

Table 18 below shows the details of the Low Power DCXO register map dealing with DCXO mode and absolute temperature readout.

Table 18. Low Power DCXO Register Detail and I²C / SPI Address Decode

Address (hexadecimal)	Address (decimal)	Bits	Access (1)	Description
0x00 – 0x02	0 - 2	[15:0]	X	NOT USED
0x03	3	[15:1]	X	NOT USED
		[0]	RW	OE CONTROL This bit is only active if the output enable function is under software control. If the device is configured for hardware control using the OE pin, writing to this bit has no effect.
0x04	4	[15:0]	RW	DIGITAL FREQUENCY CONTROL WORD 1 (LSW), **[15:0]**
0x05	5	[15:0]	RW	DIGITAL FREQUENCY CONTROL WORD 1, **[31:16]**
0x06	6	[6:0]	RW	DIGITAL FREQUENCY CONTROL WORD 1 (MSW), **[38:32]**
		[15:7]	X	NOT USED
0x07 – 0x3A	7 - 58	[15:0]	X	NOT USED
0x3B	59	[15:0]	R	ABSOLUTE TEMPERATURE READOUT (LSW), **[15:0]**
0x3C	60	[15:0]	R	ABSOLUTE TEMPERATURE READOUT, **[31:16]**
0x3D	61	[15:0]	R	ABSOLUTE TEMPERATURE READOUT, **[47:32]**
0x3E	62	[15:1]	X	NOT USED
		[0]	R	ABSOLUTE TEMPERATURE READOUT (MSB), **[48]**

Notes:
11. R = Read, W = Write, X = Don't read or write.

Register Descriptions

Register Address: 0x03. OE Control

Bit	15:1	0
Access	R	RW
Default	000000000000000b	0b
Name	NOT USED	OE[0]

Bits	Name	Access	Description
0	OE Control	RW	Output Enable Software Control. Allows the user to enable and disable the output driver via I²C. Default OFF option (datasheet code L) 0 = Output Disabled (Default) 1 = Output Enabled Default ON option (datasheet code M) 0 = Output Enabled (Default) 1 = Output Disabled This bit is only active if the Output Enable function is under software control. If the device is configured for hardware control using the OE pin, writing to this bit has no effect.

Register Address: 0x04. Digital Frequency Control Word (LSW)

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Access	RW															
Default	0000000000000000b															
Name	DIGITAL FREQUENCY CONTROL WORD [15:0]															

Bits	Name	Access	Description
15:0	DIGITAL FREQUENCY CONTROL WORD	RW	Bits [15:0] are the lower 16 bits of 39 bit FrequencyControlWord and are the Least Significant Word (LSW). The middle 16 bits are in register 0x05[15:0]. The upper 7 bits are in register 0x06[6:0] and are the Most Significant Word (MSW). All three words combined specify a 39-bit fixed point two's complement frequency control word with arithmetic format <s.38f>. Inside each row, the MSB is is stored in the highest bit index. This power-up default values of all 39 bits are 0 which sets the output frequency at its nominal value. After power-up, the system can write to these three registers to pull the frequency across the pull range. The MSW should be written last because the frequency change is initiated when the new values are loaded into the MSW. More details and examples are discussed in the previous section.

Register Address: 0x05. Digital Frequency Control Word

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Access	RW															
Default	0000000000000000b															
Name	DIGITAL FREQUENCY CONTROL WORD [31:16]															

Bits	Name	Access	Description
15:0	DIGITAL FREQUENCY CONTROL WORD	RW	Bits [15:0] are the middle 16 bits of 39 bit FrequencyControlWord *See Register Address: 0x04. Digital Frequency Control Word (LSW) for more information.*

Register Address: 0x06. Digital Frequency Control Word (MSW)

Bit	15:7	6	5	4	3	2	1	0
Access	R	RW						
Default	000000000b	0000000b						
Name	NOT USED	DIGITAL FREQUENCY CONTROL WORD [38:32]						

Bits	Name	Access	Description
6:0	DIGITAL FREQUENCY CONTROL WORD	RW	Bits [6:0] are the upper 7 bits of 39 bit FrequencyControlWord and are the Most Significant Word (MSW). *See Register Address: 0x04. Digital Frequency Control Word (LSW) for more information.*

Register Address: 0x3B. Absolute Temperature Readout (LSBs)

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Access	R															
Default	Chip temperature value															
Name	ABSOLUTE TEMPERATURE READOUT [15:0]															

Bits	Name	Access	Description
15:0	ABSOLUTE TEMPERATURE READOUT (LSW)	R	Bits [15:0] are the lower 16 bits of 49 bit AbsoluteTempReadout and are the Least Significant Word (LSW). The 2nd set of 16 bits are in register 0x3C[15:0]. The 3rd set of 16 bits are in register 0x3D[15:0]. The upper bit is in register 0x3E[0]. All four words combined specify a 49-bit fixed point two's complement frequency control word with arithmetic format «s.2i.46f>. Inside each row, the MSB is stored in the highest bit index. Inside the address table, the MSBs are stored in the higher addresses. *Usage details can be found in Temperature Readout Operation*

Register Address: 0x3C. Absolute Temperature Readout

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Access	R															
Default	Chip temperature value															
Name	ABSOLUTE TEMPERATURE READOUT [31:16]															

Bits	Name	Access	Description
15:0	ABSOLUTE TEMPERATURE READOUT	R	Bits [15:0] are the 2rd set of 16 bits of 49 bit AbsoluteTempReadout. *See Register Address: 0x3B. Absolute Temperature Readout (LSBs) for more information.*

Register Address: 0x3D. Absolute Temperature Readout

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Access	R															
Default	Chip temperature value															
Name	ABSOLUTE TEMPERATURE READOUT [47:32]															

Bits	Name	Access	Description
15:0	ABSOLUTE TEMPERATURE READOUT	R	Bits [15:0] are the 3rd set of 16 bits of 49 bit AbsoluteTempReadout. *See Register Address: 0x3B. Absolute Temperature Readout (LSBs) for more information.*

Register Address: 0x3E. Absolute Temperature Readout (MSB)

Bit	15:1	0
Access	R	R
Default	000000000000000b	Chip temperature value
Name	NOT USED	ABSOLUTE TEMPERATURE READOUT [48]

Bits	Name	Access	Description
0	ABSOLUTE TEMPERATURE READOUT (MSB)	R	Bit [0] is the MSB of the 49 bit AbsoluteTempReadout. *See Register Address: 0x3B. Absolute Temperature Readout (LSBs) for more information.*

I²C Operation

I²C Device Address Modes

There are two I²C address modes:

1. Factory Programmed Mode. The lower 4 bits of the 7-bit device address are set by ordering code as shown in Table 19. There are 16 factory programmed addresses available. In this mode, pin 5 is NC and the A0 I²C address pin control function is not available.
2. A0 Pin Control. This mode allows the user to select between two I²C Device addresses as shown in Table 20.

Addresses are specified in right-justified format. R/W bit must be added in place of LSB to complete the first byte of I²C transaction.

Table 19. Factory Programmed I²C Address Control[12]

I²C Address Ordering Code	Device I²C Address
0	0110000
1	0110001
2	0110010
3	0110011
4	0110100
5	0110101
6	0110110
7	0110111
8	0111000
9	0111001
A	0111010
B	0111011
C	0111100
D	0111101
E	0111110
F	0111111

Notes:
12. Table 19 is only valid for the DCTCXO device option which supports I²C Control and factory-programmed address.

Table 20. Pin Selectable I²C Address Control[13]

A0 Pin 5	I²C Address
0	0110010b
1	0111010b

Notes:
13. Table 20 is only valid for the DCTCXO device option which supports I²C control and A0 Device Address Control Pin.

Serial Interface Configuration Description

The ENDR-TTT includes an I²C interface to access registers that control the DCTCXO frequency pull value and provide internal temperature readout. The ENDR-TTT I²C slave-only interface supports clock speeds up to 400 kbit/s. The ENDR-TTT I²C module is based on the I²C specification, UM1024 (Rev.6 April 4, 2014 of NXP Semiconductor).

Serial Signal Format

The SDA line must be stable during the high period of the SCL. SDA transitions are allowed only during SCL low level for data communication. Only one transition is allowed during the low SCL state to communicate one bit of data. Figure 20 shows the detailed timing diagram.

An idle I²C bus state occurs when both SCL and SDA are not being driven by any master and are therefore in a logic HI state due to the pull up resistors. Every transaction begins with a START (S) signal and ends with a STOP (P) signal. A START condition is defined by a high to low transition on the SDA while SCL is high. A STOP condition is defined by a low to high transition on the SDA while SCL is high. START and STOP conditions are always generated by the master. This slave module also supports repeated START (Sr) condition which is same as START condition instead of STOP condition (the blue-color line shows repeated START in Figure 21).

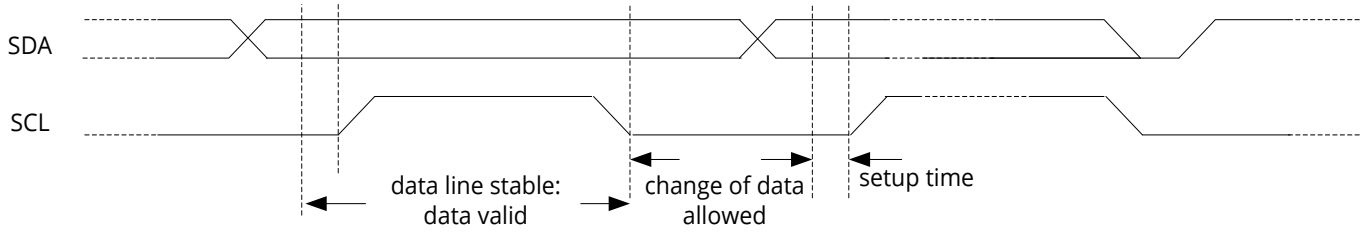


Figure 20. Data and clock timing relation in I²C bus

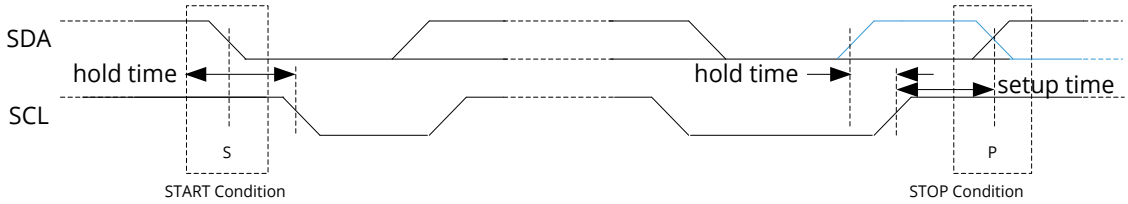


Figure 21. START and STOP (or repeated START, blue line) condition

Parallel Signal Format

Every data byte is 8 bits long. The number of bytes that can be transmitted per transfer is unrestricted. Data is transferred with the MSB (Most Significant Bit) first. The detailed data transfer format is shown in Figure 23 below.

The acknowledge bit must occur after every byte transfer and it allows the receiver to signal the transmitter that the byte was successfully received and another byte may be sent. The acknowledge signal is defined as follows: the transmitter releases the SDA line during the acknowledge clock pulse, so the receiver can pull the SDA line low and it remains stable low during the high period of this clock pulse. Setup and hold times must also be taken into account. When SDA remains high during this ninth clock pulse, this is defined as the Not-Acknowledge signal (NACK). The master can then generate either a STOP condition to abort the transfer, or a repeated START condition to start a new transfer. The only condition that leads to the generation of NACK from the ENDR-TTT is when the transmitted address does not match the slave address. When the master is reading data from the ENDR-TTT, the ENDR-TTT expects the ACK from the master at the end of received data, so that the slave releases the SDA line and the master can generate the STOP or repeated START. If there is a NACK signal at the end of the data, then the ENDR-TTT tries to send the next data. If the first bit of the next data is "0", then the ENDR-TTT holds the SDA line to "0", thereby blocking the master from generating a STOP/(re)START signal.

Parallel Data Format

This I²C slave module supports 7-bit device addressing format. The 8th bit is a read/write bit and "1" indicates a read transaction and a "0" indicates a write transaction. The register addresses are 8-bits long with an address range of 0 to 255 (00h to FFh). Auto address incrementing is supported which allows data to be transferred to contiguous addresses without the need to write each address beyond the first address. Since the maximum register address value is 255, the address will roll from 255 back to 0 when auto address incrementing is used. Obviously, auto address incrementing should only be used for writing to contiguous addresses. The data format is 16-bit (two bytes) with the most significant byte being transferred first. For a read operation, the starting register address must be written first. If that is omitted, reading will start from the last address in the auto-increment counter of the device, which has a startup default of 0x00.

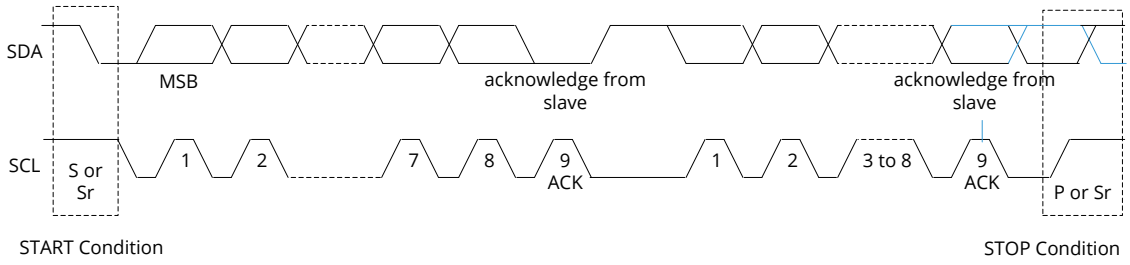


Figure 22. Parallel signaling format

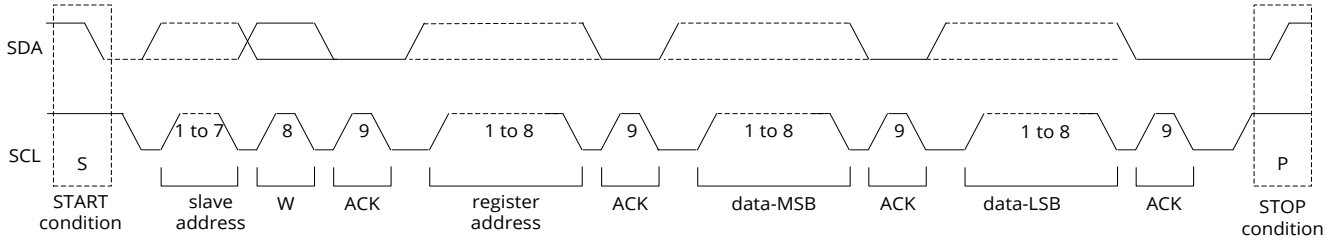


Figure 23. Parallel data byte format, write operation

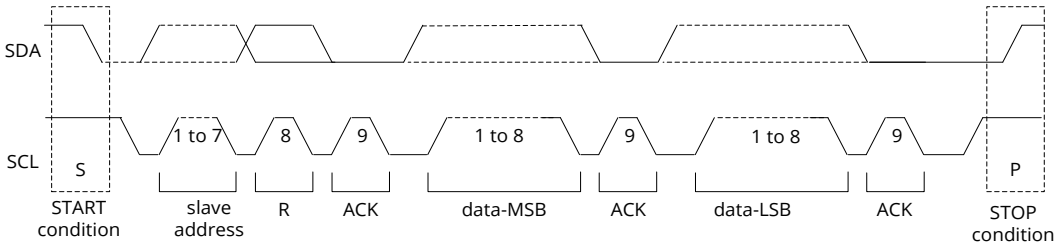


Figure 24. Parallel data byte format, read operation

Figure 25 below shows the I²C sequence for writing the 6-byte control word using auto address incrementing.

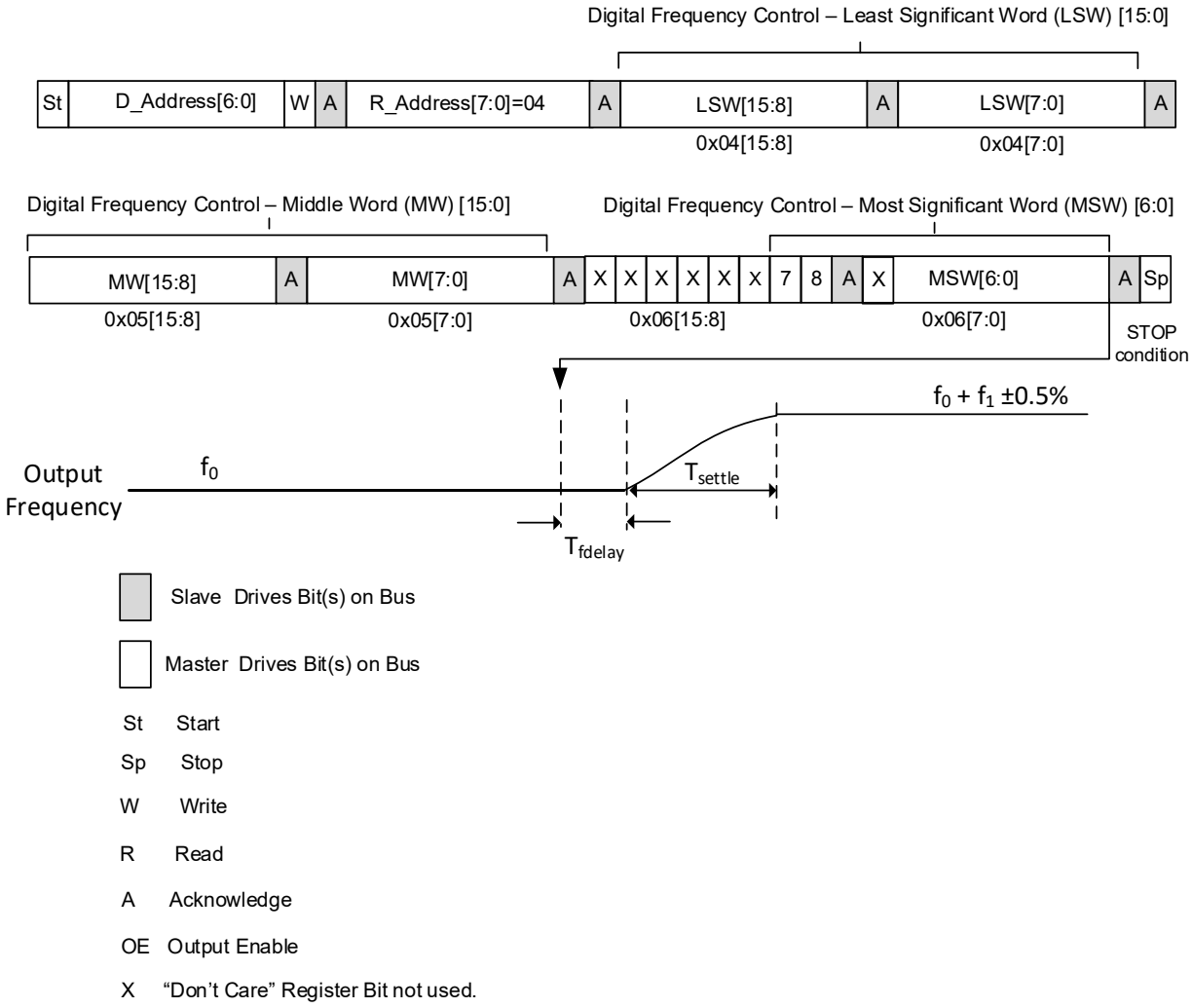


Figure 25. Writing the Frequency Control Word

Table 21. DCTCXO Delay and Settling Time

Parameter	Symbol	Minimum	Typical	Maximum	Units	Notes
Frequency Change Delay	T_{fdelay}	–	10	15	µs	Time from end of 0x01 reg MSW to start of frequency pull, as shown in Figure 25
Frequency Settling Time	T_{settle}	–	20	25	µs	Time to settle to 0.5% of frequency offset, 200 ppm frequency shift, as shown in Figure 25

I²C Timing Specification

The below timing diagram and table illustrate the timing relationships for both master and slave.

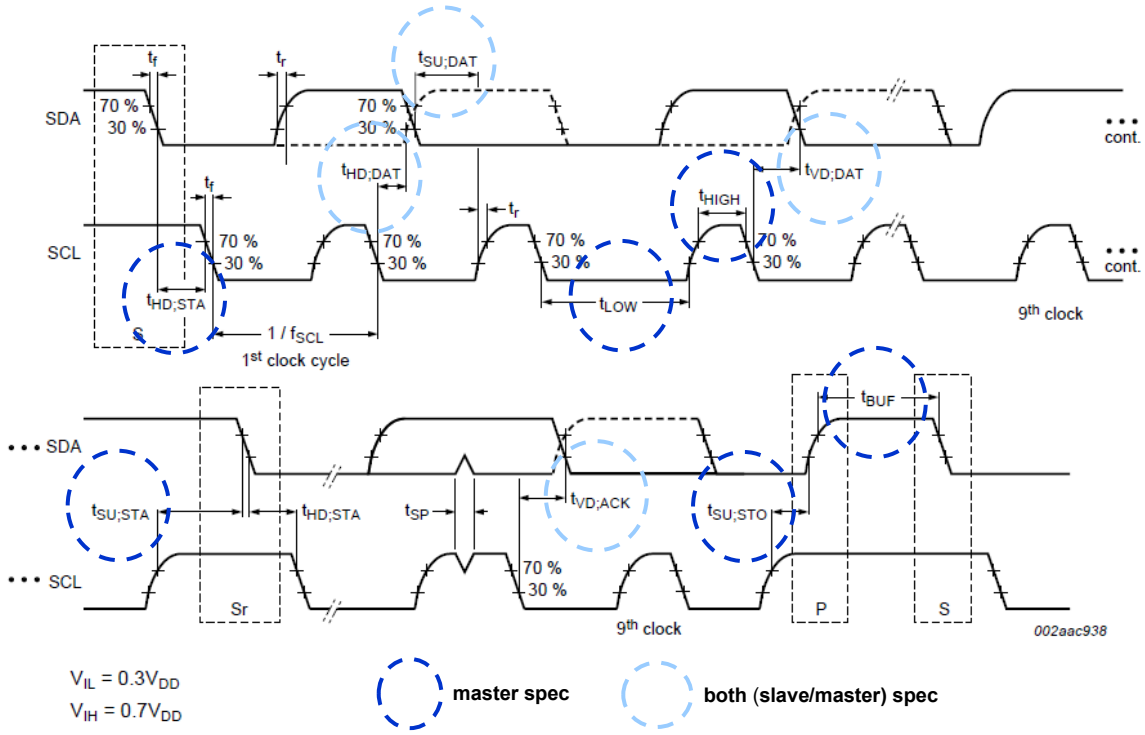


Figure 26. I²C Timing Diagram

Table 22. I²C Timing Requirements

Parameter	Speed Mode	Value	Unit
t_{SETUP}	FM+ (1 MHz)	> 50	nsec
	FM (400 KHz)	> 100	nsec
	SM (100 KHz)	> 250	nsec
t_{HOLD}	FM+ (1 MHz)	> 0	nsec
	FM (400 KHz)	> 0	nsec
	SM (100 KHz)	> 0	nsec
$t_{VD:AWK}$	FM+	> 450	nsec
	FM (400 KHz)	> 900	nsec
	SM (100 KHz)	> 3450	nsec
$t_{VD:DAT}$		NA (s-awk + s-data)/(m-awk/s-data)	

SPI Operation

SPI (Serial Peripheral Interface) is a 4-pin synchronous serial protocol that allows a master device to initiate half-duplex communication with one or more slave devices. The pin functions are as follows:

SCLK: Serial Clock which supports up to 5 MHz operating frequency.

MOSI: Master Output Slave Input. This is the data input pin to the ENDR-TTT and is used by the master to write data to the ENDR-TTT control registers.

MISO: Master Input Slave Output. This is the data output pin of the ENDR-TTT and is used by the master to read data from the ENDR-TTT control registers.

$\overline{SS}$: Active Low SPI Chip Select. This pin is used by the master to select the ENDR-TTT as the active slave device on the SPI bus. When the master drives the ENDR-TTT pin low, the ENDR-TTT is selected as the target of a read or write transaction.

The following Figure 27 illustrates the logical connection between one SPI master and 3 SPI slaves. Note that this diagram is shows only an example logical connection and is not a detailed schematic intended to show pull-up resistors and other components which may also be required.

There are two allowed states for idle SCLK state, HI and LOW and these states are called clock phase. There are also two modes for clock sampling edge, rising edge and falling edge and these modes are called clock polarity. Since there are two allowed clock phases and two allowed clock polarities, this means there are four total modes of SPI operation as illustrated below in Figure 28.

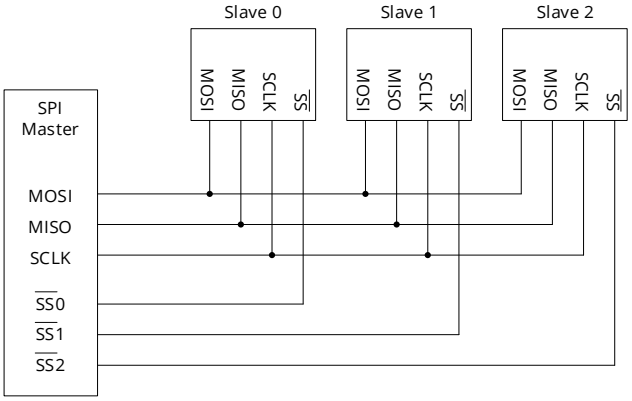


Figure 27. Multi-slave SPI bus connections

Mode	SCLK Polarity SCLK_POL	SCLK Phase SCLK_PHA
Mode 0	Low At Start	Rising Edge
Mode 1	Low At Start	Falling Edge
Mode 2	High At Start	Falling Edge
Mode 3	High At Start	Rising Edge

Figure 28. SPI operation modes

The ENDR-TTT supports modes 1 and 2.

The serial byte interface format is shown below: 8-bit command (read or write), 8-bit SPI address and 16-bit data.

The serial order is most significant bit (MSB) first. The SPI protocol also supports auto address incrementing which means the address will automatically increment after the first transaction. Auto address incrementing will result in higher data throughput when writing to registers with contiguous addresses. If it is required to write to non-contiguous addresses, a write command and register address must be used for each transaction after the delay (125 us min). Without such delay, the device will consider command and address bytes as a data for the consequent register.

The detail register descriptions are covered in the I²C/SPI Control Registers.

A description of DCO control is in DCO Functional Description and a description of changing the output center frequency is in any-frequency Functional Description.

The below Figure 30 shows the timing diagram for modes 0 and 3.

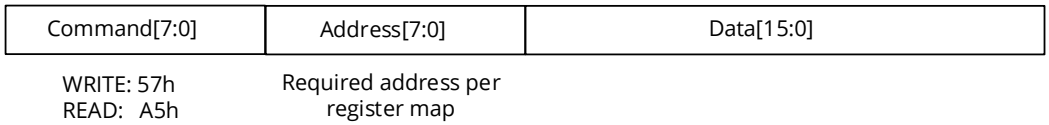


Figure 29. SPI control word format

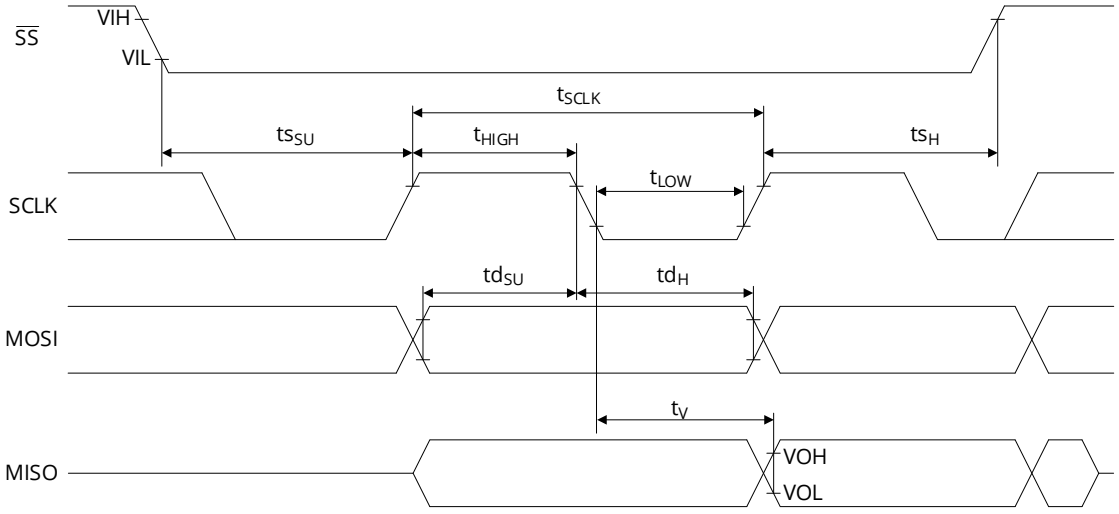


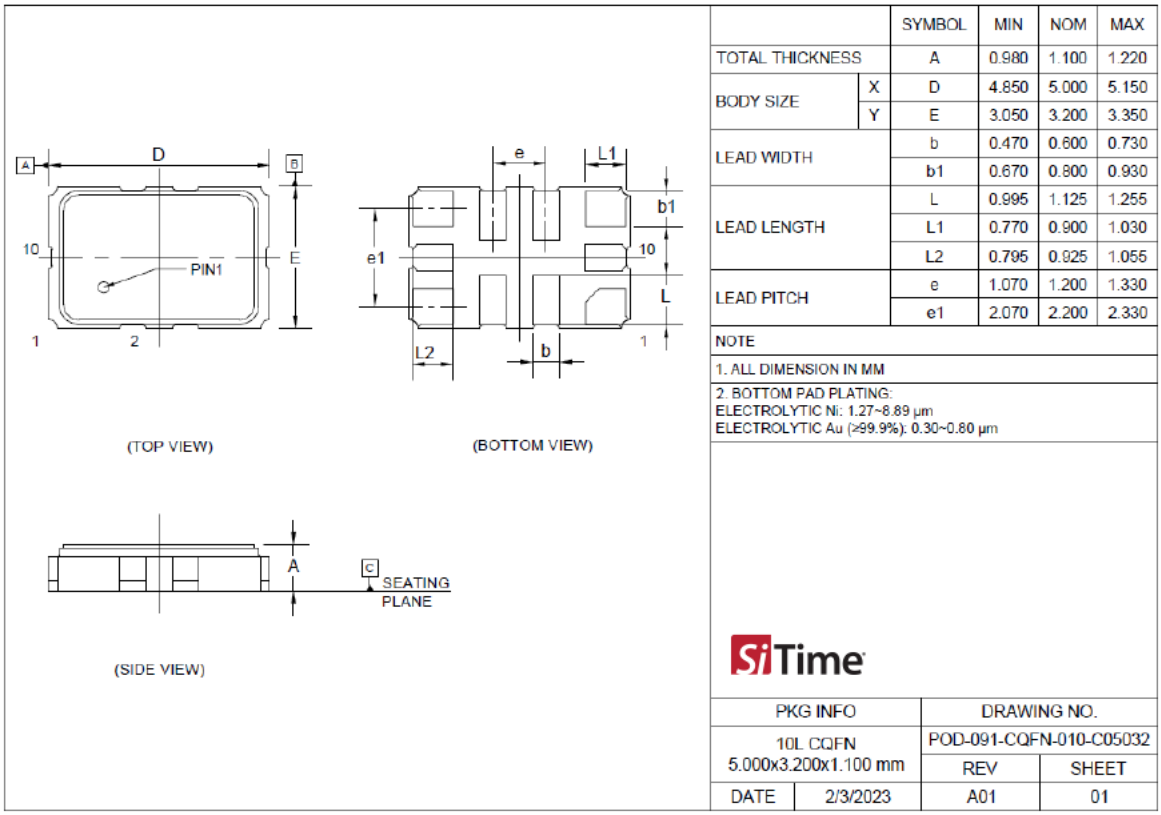
Figure 30. SPI Timing Diagram (Mode 1/2)

Table 23. SPI Timing Requirements

Parameter	Symbol	Min.	Typ.	Max.	Unit
Setup time for MOSI to SCLK Falling Edge	td_{SU}	28	–	–	ns
Hold time for MOSI to SCLK Falling edge	td_{H}	1	–	–	ns
Time from active edge of SCLK clock to valid MISO data available at pin	t_{v}	–	–	30	ns
Period of SCLK	t_{SCLK}	–	–	200	ns
High Width of SCLK	t_{HIGH}	–	$t_{SCLK}/2$	–	ns
Low Width of SCLK	t_{LOW}	–	$t_{SCLK}/2$	–	ns
Setup time for SSB falling edge to SCLK rising edge	ts_{SU}	$1.5*t_{SCLK}$	–	–	ns
Hold time from SSB rising edge to SCLK rising edge	ts_{H}	$1.5*t_{SCLK}$	–	–	ns

Dimensions and Patterns

Package Size – Dimensions (Unit: mm)

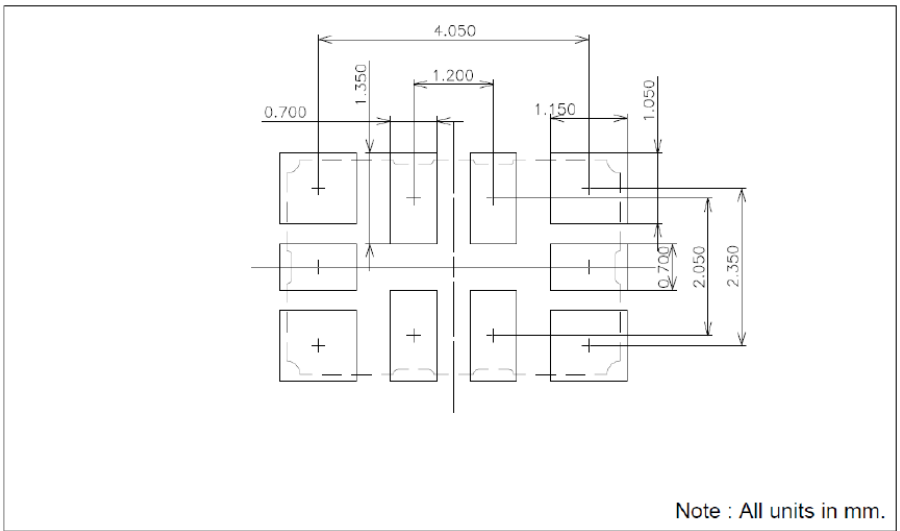


		SYMBOL	MIN	NOM	MAX
TOTAL THICKNESS		A	0.980	1.100	1.220
BODY SIZE	X	D	4.850	5.000	5.150
	Y	E	3.050	3.200	3.350
LEAD WIDTH		b	0.470	0.600	0.730
		b1	0.670	0.800	0.930
LEAD LENGTH		L	0.995	1.125	1.255
		L1	0.770	0.900	1.030
		L2	0.795	0.925	1.055
LEAD PITCH		e	1.070	1.200	1.330
		e1	2.070	2.200	2.330

NOTE
1. ALL DIMENSION IN MM
2. BOTTOM PAD PLATING:
ELECTROLYTIC Ni: 1.27~8.89 µm
ELECTROLYTIC Au (≥99.9%): 0.30~0.80 µm

PKG INFO		DRAWING NO.	
10L CQFN 5.000x3.200x1.100 mm		POD-091-CQFN-010-C05032	
		REV	SHEET
DATE	2/3/2023	A01	01

Recommended Land Pattern (Top View)



Note : All units in mm.

	PKG INFO	SPL DRAWING NO.	
	10L CQFN 5.000x3.200 mm	SPL-091-CQFN-010-C05032	
DATE		REV	SHEET
2023/02/03		A01	01

Pb-free, Halogen-free, Antimony-free, RoHS and REACH compliant

Layout Guidelines

- ENDR-TTT uses internal regulators to minimize the impact of power supply noise. For further noise reduction, it is essential to use two bypass capacitors (0.1 µF and 10 µF). Place the 0.1 µF capacitor as close to the VDD pin as possible, typically within 1 mm to 2 mm. Place the 10 µF capacitor within 2 inches of the device VDD and VSS pins.
- It is also recommended to connect all NC pins to the ground plane and place multiple vias under the GND pin for maximum heat dissipation.
- For additional layout recommendations, refer to the Best Design Layout Practices.

Manufacturing Guidelines

ENDR-TTT Super-TCXOs are precision timing devices. **Proper PCB solder and cleaning processes** must be followed to ensure best performance and long-term reliability.

- **No Ultrasonic or Megasonic Cleaning:** Do not subject ENDR-TTT to an ultrasonic or megasonic cleaning environment. Otherwise, permanent damage or long-term reliability issues to the device may result.
- **No external cover.** Unlike legacy quartz TCXOs, ENDR-TTT is engineered to operate reliably, without performance degradation in the presence of ambient disturbers such as airflow and sudden temperature changes. Therefore, the use of an external cover typically required by quartz TCXOs is not needed.
- **Reflow profile:** For mounting these devices to the PCB, IPC/JEDEC J-STD-020 compliant reflow profile must be used. Device performance is not guaranteed if soldered manually or with a non-compliant reflow profile.
- **PCB cleaning:** After the surface mount (SMT)/reflow process, solder flux residues may be present on the PCB and around the pads of the device. Excess residual solder flux may lead to problems such as pad corrosion, elevated leakage currents, increased frequency aging, or other performance degradation. For optimal device performance and long-term reliability, thorough cleaning to remove all the residual flux and drying of the PCB is required as shortly after the reflow process as possible. Water soluble flux is recommended. In addition, it is highly recommended to avoid the use of any “no clean” flux. However, if the reflow process necessitates the use of “no clean” flux, then utmost care should be taken to remove all residual flux between SiTime device and the PCB. Note that ultrasonic PCB cleaning should not be used with SiTime oscillators.

For additional manufacturing guidelines and marking/tape-reel instructions, refer to SiTime Manufacturing Notes.

Additional Information

Table 24. Additional Information

Document	Description	Download Link
ECCN #: EAR99	Five character designation used on the commerce Control List (CCL) to identify dual use items for export control purposes.	—
HTS Classification Code: 8542.39.0000	A Harmonized Tariff Schedule (HTS) code developed by the World Customs Organization to classify/define internationally traded goods.	—
Evaluation Boards	SiT6726EBB-L for Regulated LVCMOS output SiT6726EBB-C for Clipped Sine output	Contact SiTime
Manufacturing Notes	Tape & Reel dimension, reflow profile and other manufacturing related info	https://www.sitime.com/support/resource-library/manufacturing-notes-sitime-products
Qualification Reports	RoHS report, reliability reports, composition reports	In progress
Performance Reports	Additional performance data such as phase noise, current consumption and jitter for selected frequencies	In progress
Termination Techniques	Termination design recommendations	http://www.sitime.com/support/application-notes
Layout Techniques	Layout recommendations	http://www.sitime.com/support/application-notes

Revision History

Table 25. Revision History

Version	Release Date	Change Summary
0.91	29-Oct-2025	ENDR-TTT Initial release
0.99	27-Feb-2026	Pre-Production Release
1.0	26-Jun-2026	Production Release

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